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aPisa2_1A Schematics Document

HASWELL INTEL LYNX POINT(ULT)

~ aPisa2 195" UMA SKU : U,N,P
 % aPisa2 195" GPU SKU : U,N,O,G
 ~~~~~  
 & aPisa2 23" UMA SKU : S,A,P  
 \$ aPisa2 23" GPU SKU : S,A,O,G


R: Unmount  
 S: Scalar  
 G: GPU  
 U: UMA(NOT S)  
 A: AMP  
 N: non AMP  
 P: PCIE Half Card(non GPU)  
 O: OCP

OCP BOM manual control:  
 R1360 R1361,R1362,R1363 [63.R0031.16L]  
 Mount by BOM change list when w/o OCP

GPU SKU:  
 Hynix H5TC2G63FFR-11C  
 R7419=8.45K(64.84515.6DL)

Samsung K4W2G1646E-BC11  
 Hynix H5TQ2G63DFR-11C  
 R7419=4.53K(64.45315.6DL)

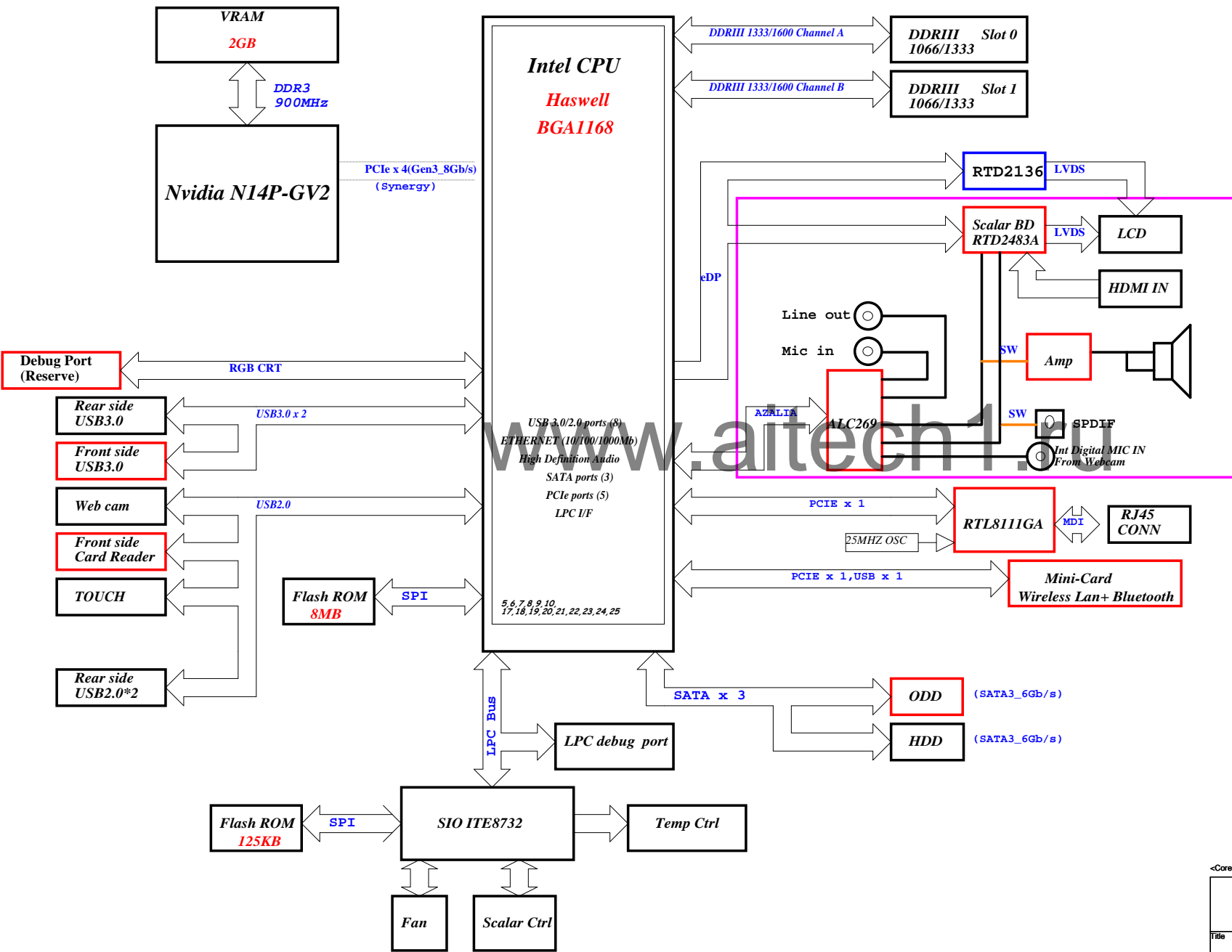
Project code :91.3MS01.001  
 PCB No :13038  
 Revision :1A  
 Project Name :PIM86L/aPisa2  
 Size : 150x240mm

|                                                                                                                                                                                                   |                                  |                  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|------------------|
| <Core Design>                                                                                                                                                                                     |                                  |                  |
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aPisa2 Block Diagram (GPU)

Project code :91.3KF01.001  
PCB No :13038  
Revision :SA  
Project Name :APISA2



| SYSTEM DC/DC<br>RT8223MGQW 31   |                                                  |
|---------------------------------|--------------------------------------------------|
| INPUTS                          | OUTPUTS                                          |
| DCBATOUT                        | 5V_AUX_S5<br>3D3V_AUX_S5<br>5V_Charger<br>3D3V_A |
| CPU DC/DC<br>ISL95832HRTZ 32-33 |                                                  |
| INPUTS                          | OUTPUTS                                          |
| DCBATOUT                        | VCC_CORE                                         |
| SYSTEM DC/DC<br>ISL95832HRTZ 34 |                                                  |
| INPUTS                          | OUTPUTS                                          |
| DCBATOUT                        | VCC_GFXCORE                                      |
| SYSTEM DC/DC<br>ISL95870BHRZ 35 |                                                  |
| INPUTS                          | OUTPUTS                                          |
| DCBATOUT                        | 1D05V_VTT                                        |
| SYSTEM DC/DC<br>TPS51116RGER 36 |                                                  |
| INPUTS                          | OUTPUTS                                          |
| DCBATOUT                        | 1D5V_S3<br>0D75V_S0<br>DDR_VREF_S3               |
| LDO<br>RT9025-25PSP 37          |                                                  |
| INPUTS                          | OUTPUTS                                          |
| 3D3V_S0                         | 1D8V_S0                                          |
| SYSTEM DC/DC<br>TPS51461RGER 38 |                                                  |
| INPUTS                          | OUTPUTS                                          |
| 5V_S5                           | 0D85V_S0                                         |
| PCB LAYER                       |                                                  |
| L1:Top<br>L2:VCC<br>L3:Signal   | L4:Signal<br>L5:GND<br>L6:Bottom                 |

<Core Design>



## PCH Strapping Huron River Schematic Checklist Rev.0\_7

| Name                                         | Schematics Notes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPKR                                         | <b>Reboot option at power-up</b><br><b>Default Mode:</b> Internal weak Pull-down.<br><b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ<br>- 10-kΩ weak pull-up resistor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| INIT3_3V#                                    | Weak internal pull-up. Leave as "No Connect".                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GNT3#/GPIO55<br>GNT2#/GPIO53<br>GNT1#/GPIO51 | GNT[3:0]# functionality is not available on Mobile.<br>Mobile: Used as GPIO only<br>Pull-up resistors are not required on these signals.<br>If pull-ups are used, they should be tied to the Vcc3_3power rail.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| SPI_MOSI                                     | <b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-k? weak pull-up resistor.<br><b>Disable Danbury:</b> left floating, no pull-down required.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| NV_ALE                                       | <b>Enable Danbury:</b> Connect to +NVRAM_VCCQ with 8.2-kohm<br>weak pull-up resistor [CRB has it pulled up<br>with 1-kohm no-stuff resistor]<br><b>Disable Danbury:</b> leave floating (internal pull-down)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| NC_CLE                                       | DMI termination voltage. Weak internal pull-up. Do not pull low.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| HAD_DOCK_EN#<br>/GPIO[33]                    | Low (0) - Flash Descriptor Security will be overridden. Also,<br>when this signals is sampled on the rising edge of PWROK<br>then it will also disable Intel ME and its features.<br>High (1) - Security measure defined in the Flash Descriptor will be enabled.<br>Platform design should provide appropriate pull-up or pull-down depending on<br>the desired settings. If a jumper option is used to tie this signal to GND as<br>required by the functional strap, the signal should be pulled low through a weak<br>pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently.<br>Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal<br>pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for<br>strapping functions. |
| HDA_SDO                                      | Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| HDA_SYNC                                     | Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GPIO15                                       | Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no<br>confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher<br>suite with confidentiality<br>Note : This is an un-muxed signal.<br>This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low.<br>Sampled at rising edge of RSMRST#.<br>CRB has a 1-kohm pull-up on this signal to +3.3VA rail.                                                                                                                                                                                                                                                                                                                                               |
| GPIO8                                        | GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down<br>using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of<br>RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is<br>enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| GPIO27                                       | <b>Default = Do not connect (floating)</b><br>High(1) = Enables the internal VccVRM to have a clean supply for<br>analog rails. No need to use on-board filter circuit.<br>Low (0) = Disables the VccVRM. Need to use on-board filter<br>circuits for analog rails.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

## Processor Strapping Huron River Schematic Checklist Rev.0\_7

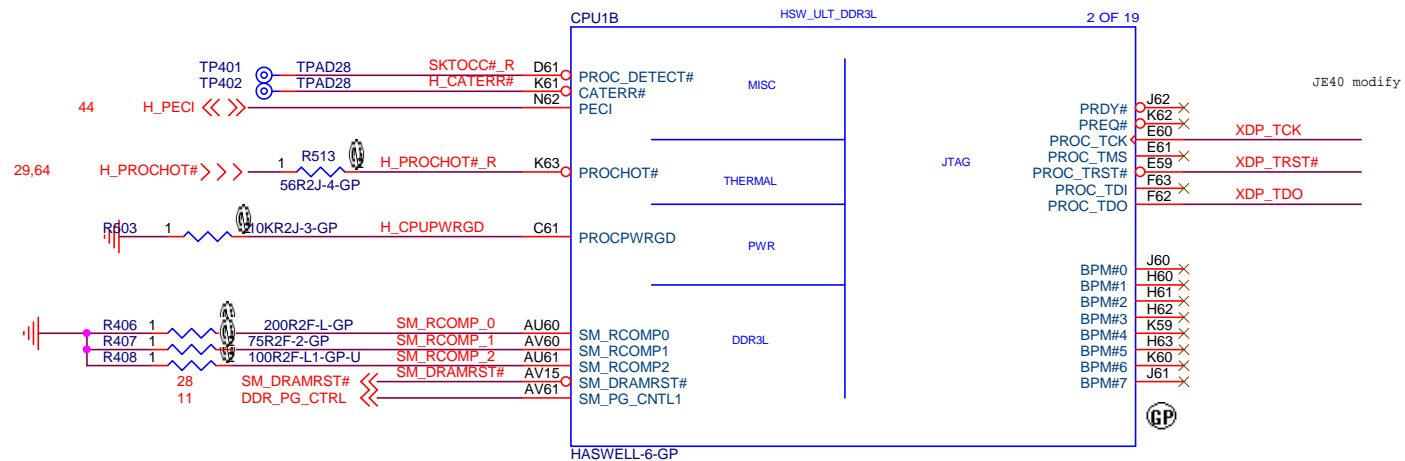
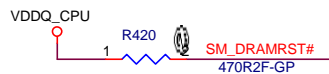
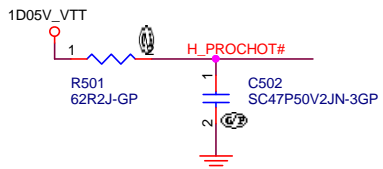
| Pin Name | Strap Description                                  | Configuration (Default value for each bit is<br>1 unless specified otherwise)                                                                                                                                                                                                         | Default<br>Value |
|----------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| CFG[2]   | <b>PCI-Express Static<br/>Lane Reversal</b>        | <b>1:</b> Normal Operation.<br><b>0:</b> Lane Numbers Reversed 15 -> 0, 14 -> 1, ...                                                                                                                                                                                                  | 1                |
| CFG[4]   |                                                    | Disabled - No Physical Display Port attached to<br><b>1:</b> Embedded DisplayPort.<br>Enabled - An external Display Port device is<br><b>0:</b> connected to the EMBEDDED display Port                                                                                                | 0                |
| CFG[6:5] | <b>PCI-Express<br/>Port Bifurcation<br/>Straps</b> | <b>11 :</b> x16 - Device 1 functions 1 and 2 disabled<br><b>10 :</b> x8, x8 - Device 1 function 1 enabled ;<br>function 2 disabled<br><b>01 :</b> Reserved - (Device 1 function 1 disabled ;<br>function 2 enabled)<br><b>00 :</b> x8, x4, x4 - Device 1 functions 1 and 2<br>enabled | 11               |
| CFG[7]   | <b>PEG DEFER TRAINING</b>                          | <b>1:</b> PEG Train immediately following xxRESETB de assertion<br><b>0:</b> PEG Wait for BIOS for training                                                                                                                                                                           |                  |

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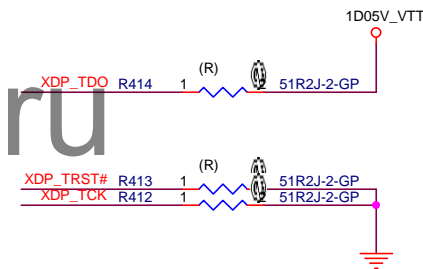
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| <b>Table of Content</b>                                                       |                                  |                            |    |
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5  
SSID = CPU



71.HASWE.G0U



2013/03/04 CHANGE TO ONE CHIP\_Ryan

## <Core Design>

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**CPU (THERMAL/CLOCK/PM)**

|        |  |
|--------|--|
| Size   |  |
| Custom |  |

Document Number

**aPISA2**

|     |    |
|-----|----|
| Rev | 1A |
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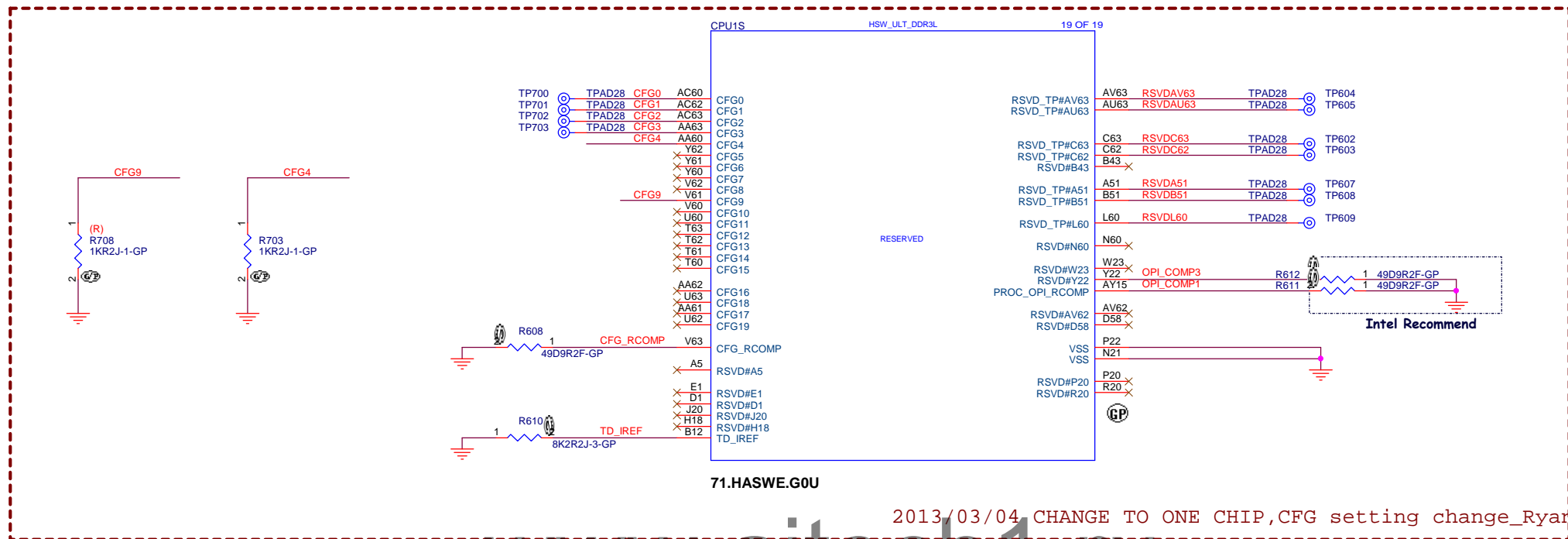
Sheet 4 of 73







SSID = CPU



## 6.3 Reset and Miscellaneous Signals

Table 30. Reset and Miscellaneous Signals

| Signal Name | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Direction / Buffer Type |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|
| CFG[19:0]   | <b>Configuration Signals:</b><br>The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none"><li>• <b>CFG[3:0]:</b> Reserved configuration lane. A test point may be placed on the board for these lanes.</li><li>• <b>CFG[4]: eDP enable</b><ul style="list-style-type: none"><li>— 1 = Disabled</li><li>— 0 = Enabled</li></ul></li><li>• <b>CFG[19:5]:</b> Reserved configuration lanes. A test point may be placed on the board for these lands.</li></ul> | I/O<br>GTL              |
| CFG_RCOMP   | Configuration resistance compensation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                         |
| FC_x        | FC (Future Compatibility) signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.                                                                                                                                                                                                                                                                                                                                                                              |                         |

## 7.4

### Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD\_TP – these signals should be routed to a test point
- RSVD\_NCTF – these signals are non-critical to function and may be left unconnected

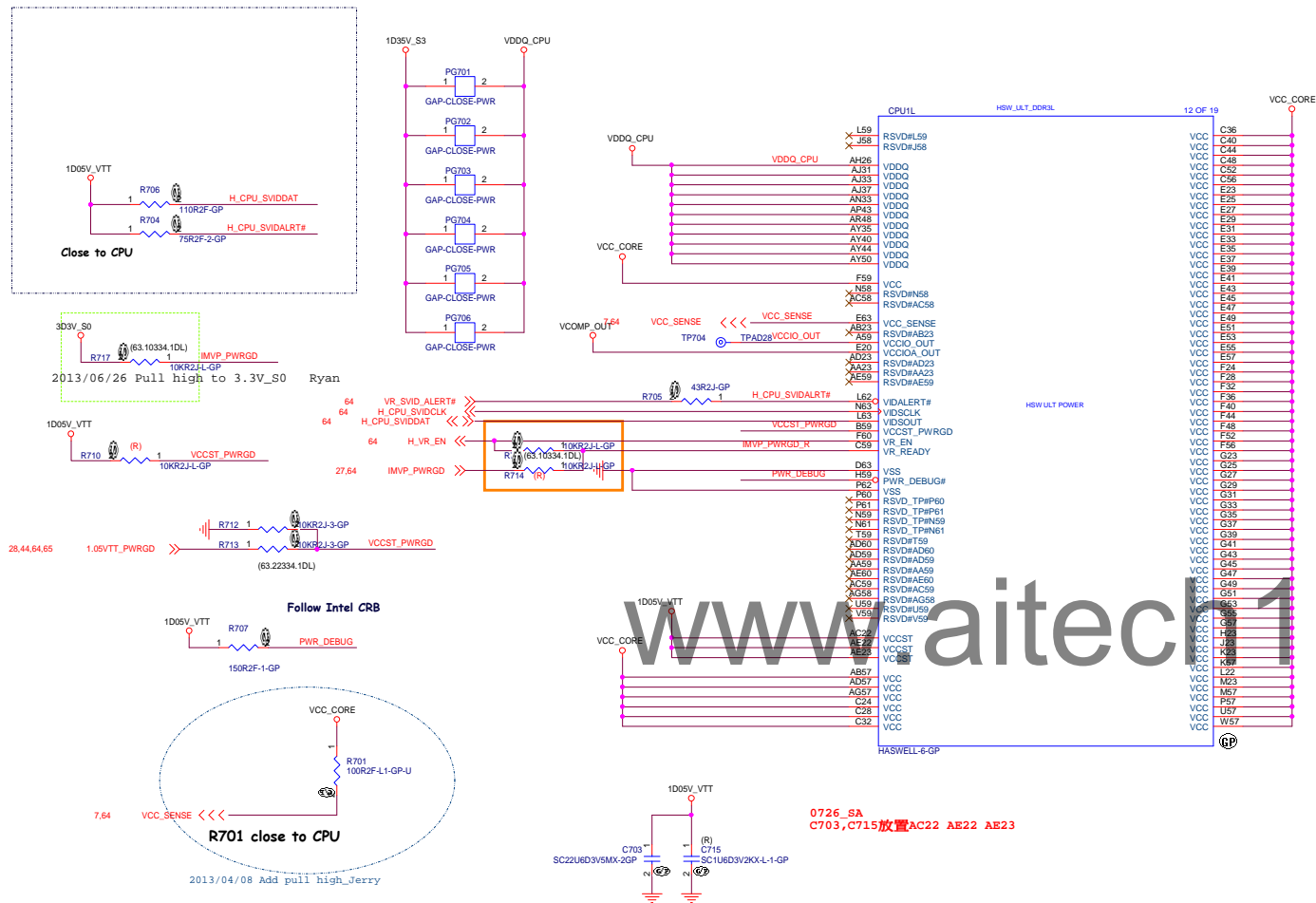
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Title  
**CPU (RESERVED)**  
Size B Document Number  
**aPISA2** Rev  
**1A**  
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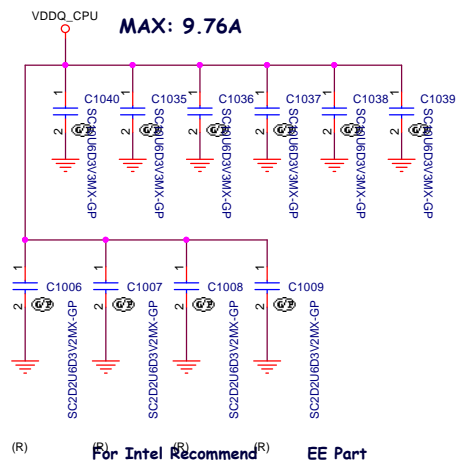


SSID = CPU



2013/03/04 CHANGE TO ONE CHIP\_Ryan





2013/03/18 ADD CAP FOR CPU\_Ryan

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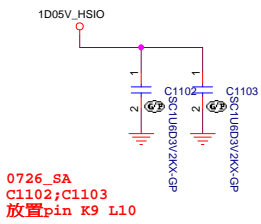
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| CPU (POWER CAP1) |                           |                                                                               |               |
| Size             | Document Number           |                                                                               | Rev           |
| A3               | aPISA2                    |                                                                               | 1A            |
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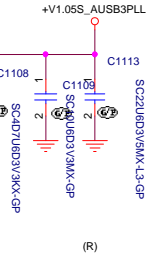
0726\_SA 擺放電容的位置請參考Page 21  
每個位置如下

MAX: 1.92A

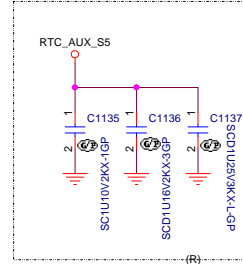
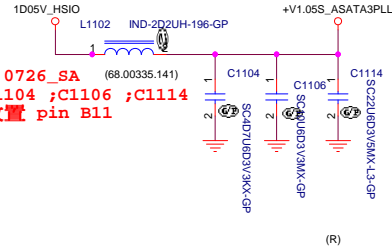
0726\_SA-DI C1137



0726\_SA  
C1108 ;C1109 ;C1113  
放置 pin B18

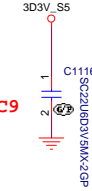


0726\_SA  
C1104 ;C1106 ;C1114  
放置 pin B11



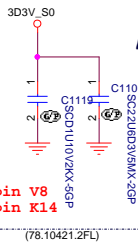
0726\_SA  
C1135;C1136;C1137  
放置 pin AG10

0726\_SA  
C1116放置 pin AC9

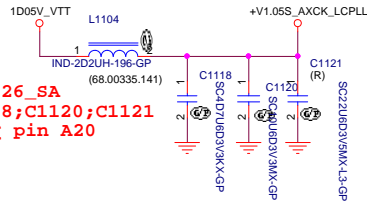


MAX: 0.285A

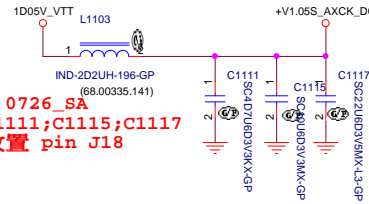
0726\_SA  
C1101 放置 pin V8  
C1119 放置 pin K14



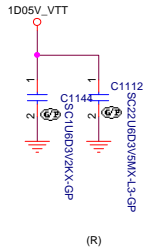
0726\_SA  
C1118;C1120;C1121  
放置 pin A20



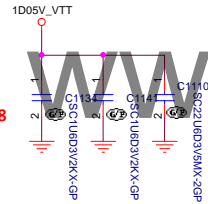
0726\_SA  
C1111;C1115;C1117  
放置 pin J18



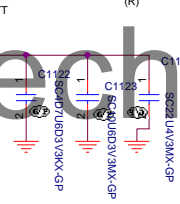
0726\_SA  
C1144;C1112  
放置 pin AE9



0726\_SA  
C1110 放置 pin J11  
C1134 C1141 放置 pin J11, AE8



0726\_SA  
C1122;C1123;C1124  
放置 pin AA21



2013/03/18 ADD CAP FOR CPU\_Ryan

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CPU (POWER CAP2)

Size  
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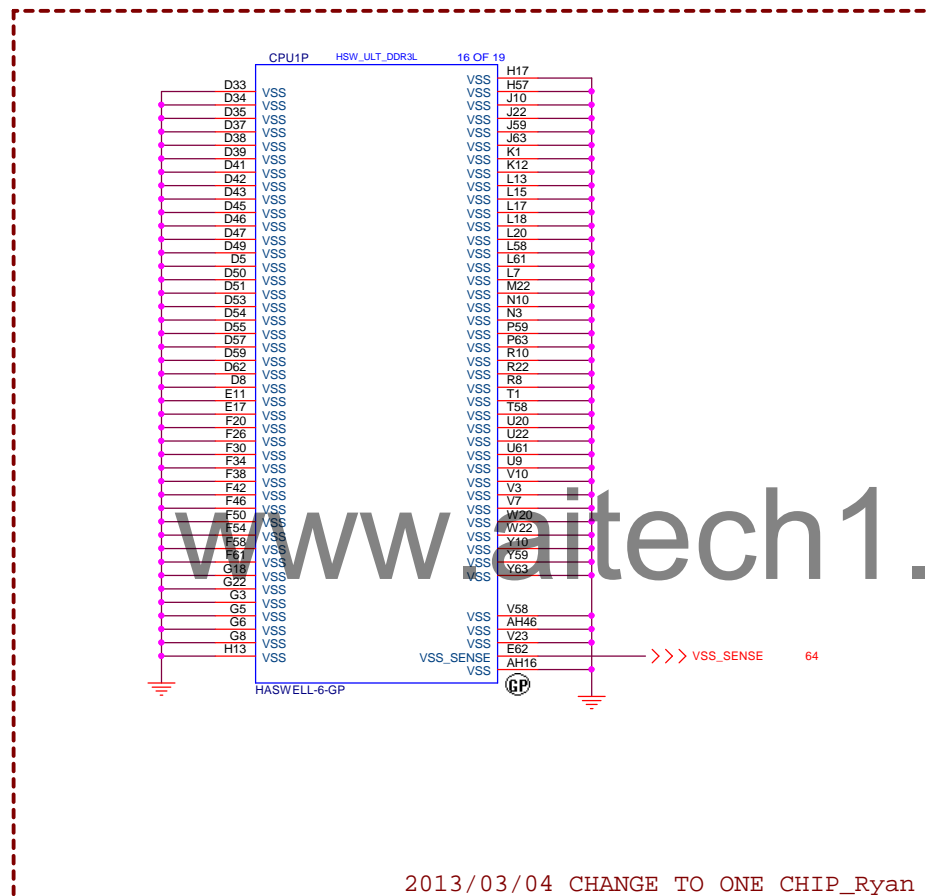
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Rev  
1A



SSID = CPU

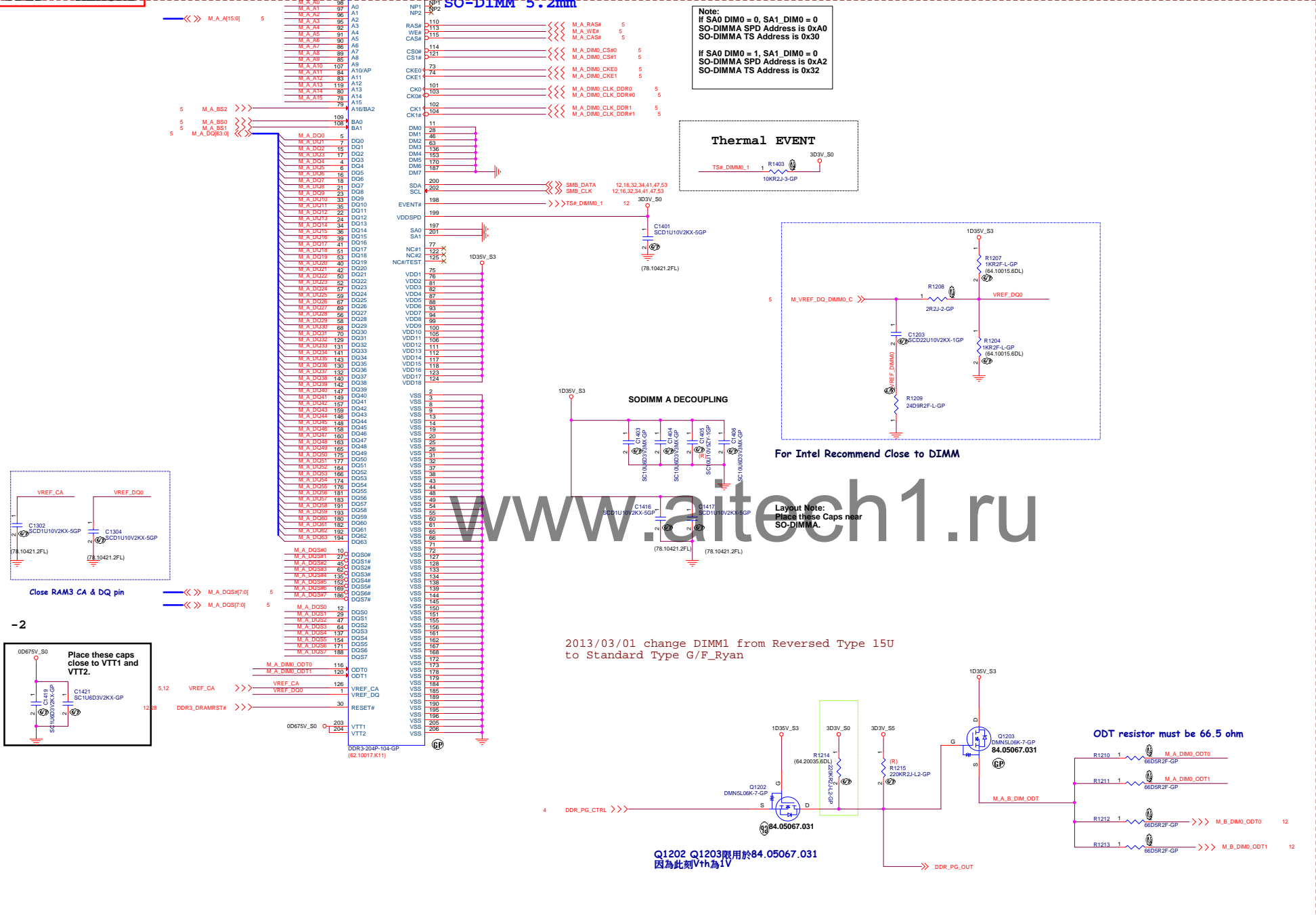


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| A3                                                                         | aPISA2                    | 1A                  |          |
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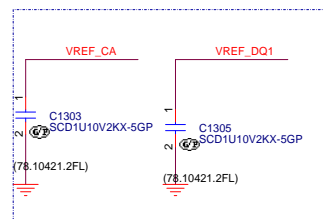
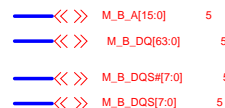


SSID = MEMORY

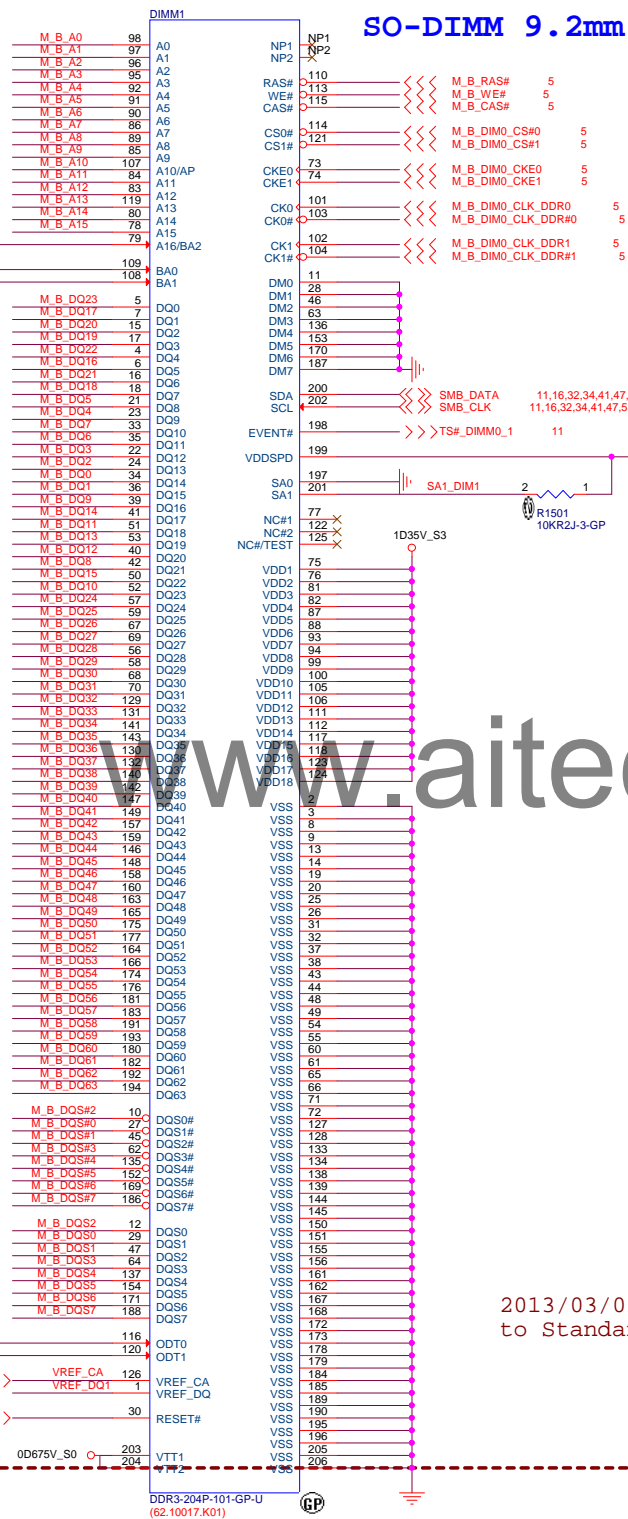
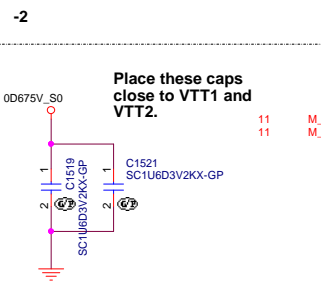




**SSID = MEMORY**

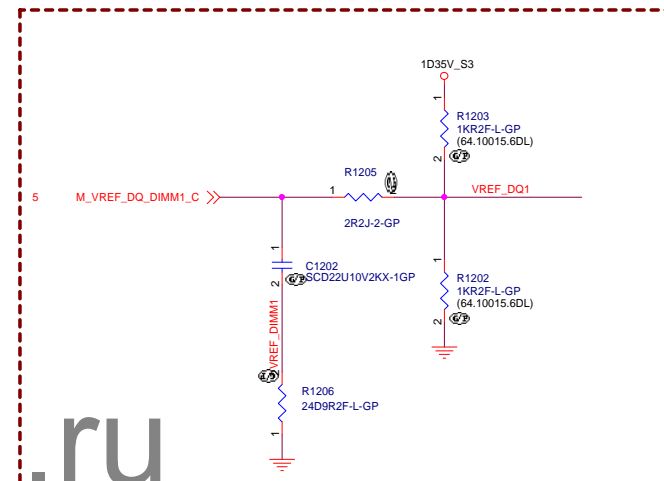


Close RAM3 CA & DQ pin

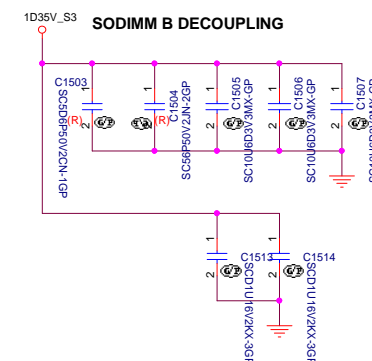


**Note:**  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

**SO-DIMMB is placed farther from the Processor than SO-DIMMA**



2013/03/11 For Intel Recommend Close to DIMM\_Ryan



**Layout Note:**  
Place these Caps near  
SO-DIMMB.

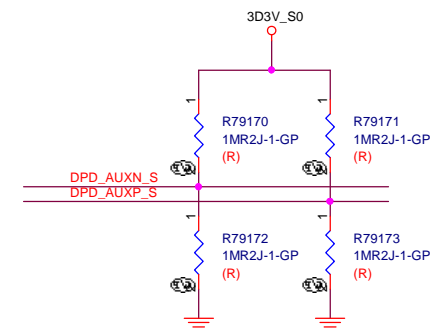
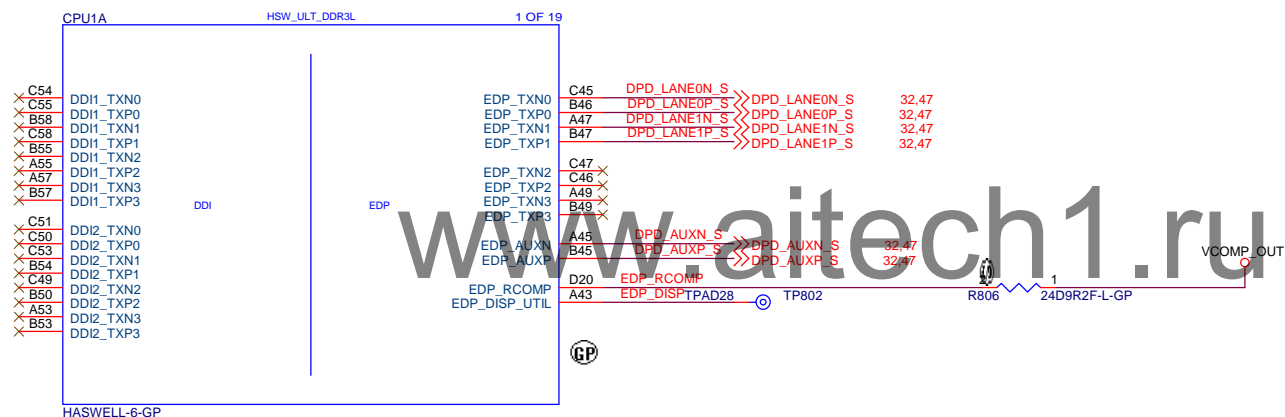
2013/03/01 change DIMM2 from Reversed Type 15U to Standard Type G/F\_Ryan

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Taipei Hsien 221, Taiwan, R.O.C.

|                     |                           |             |           |
|---------------------|---------------------------|-------------|-----------|
| Title               |                           |             |           |
| <b>DDR3-SODIMM2</b> |                           |             |           |
| Size Custom         | Document Number           |             | Rev       |
|                     | <b>aPISA2</b>             |             | <b>1A</b> |
| Date                | Thursday, August 29, 2013 | Sheet 12 of | 73        |





2013/03/07 CHANGE TO ONE CHIP\_Ryan

<Core Design>

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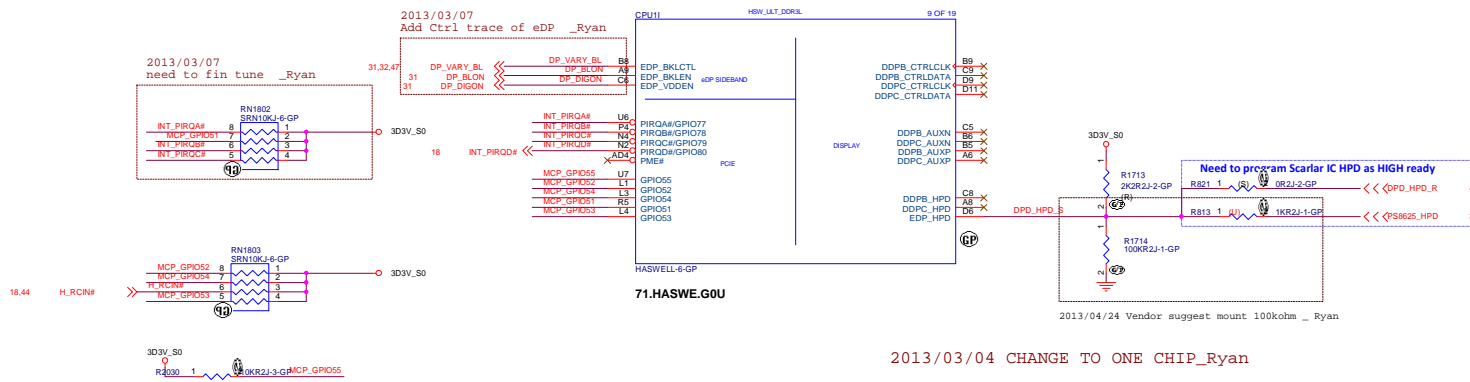
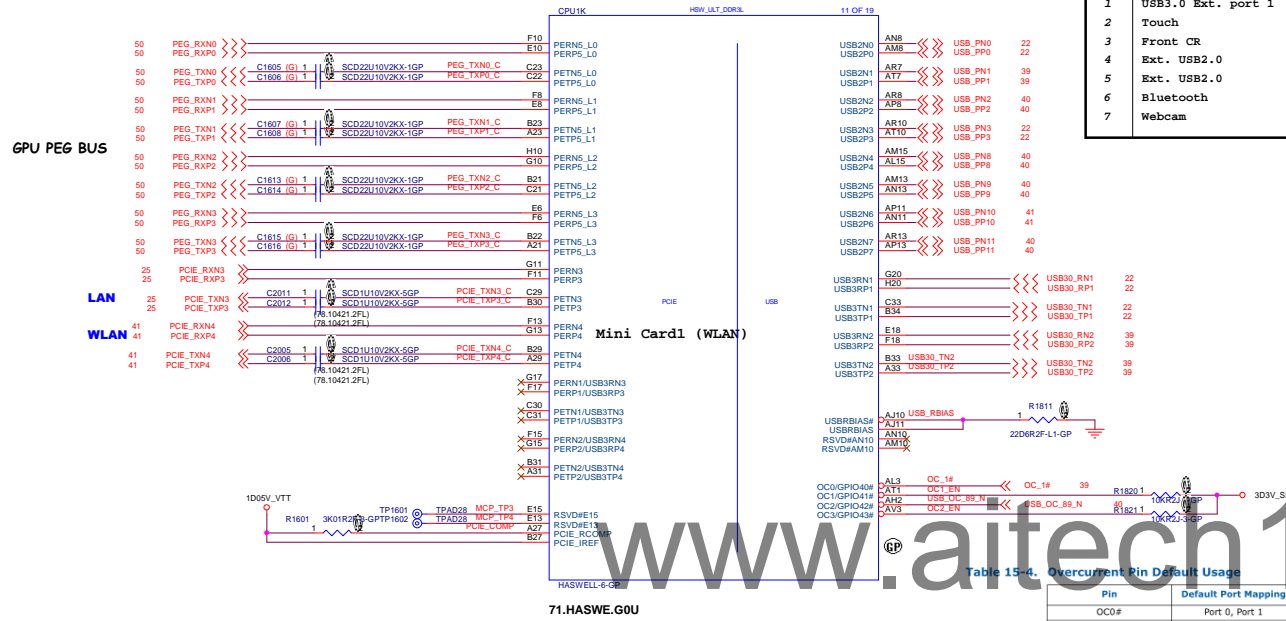
|                                 |                 |     |
|---------------------------------|-----------------|-----|
| Title                           |                 |     |
| CPU (DDI/EDP)                   |                 |     |
| Size B                          | Document Number | Rev |
|                                 | aPISA2          | 1A  |
| Date: Thursday, August 29, 2013 | Sheet 13 of 73  |     |



SSID = PCH

## USB Table

| Pair | Device                   |
|------|--------------------------|
| 0    | Front USB3.0 Ext. port 2 |
| 1    | USB3.0 Ext. port 1       |
| 2    | Touch                    |
| 3    | Front CR                 |
| 4    | Ext. USB2.0              |
| 5    | Ext. USB2.0              |
| 6    | Bluetooth                |
| 7    | Webcam                   |



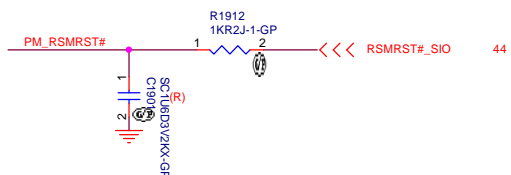
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

| CPU (PCI / USB / NVRAM) |                           |                |
|-------------------------|---------------------------|----------------|
| File                    | Document Number           | Rev            |
| Size                    | aPISA2                    | 1A             |
| Date                    | Thursday, August 29, 2013 | Sheet 14 of 73 |

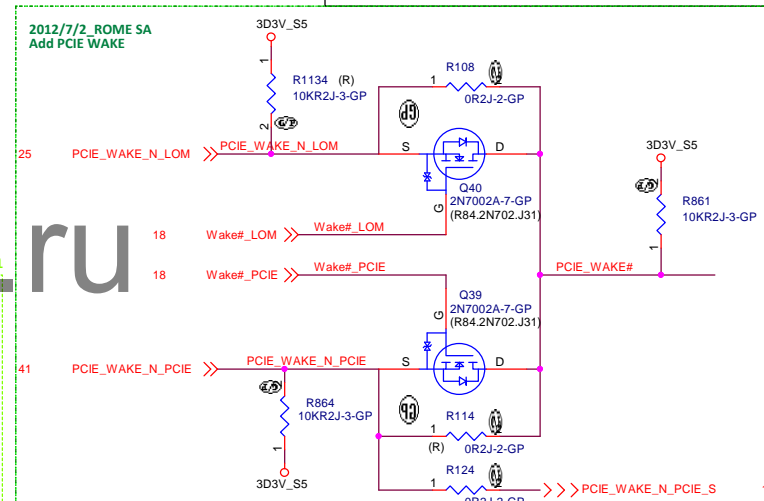
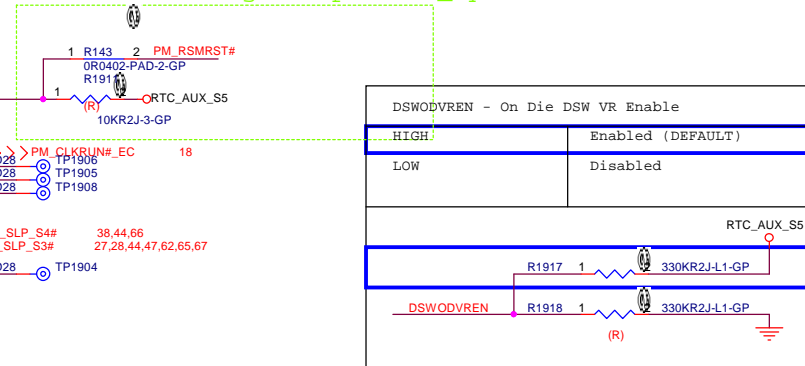


Signal Routing Guideline:  
DMI\_ZCOMP keep W=4 mils and  
routing length less than 500  
mils.  
DMI\_IRCOMP keep W=4 mils and  
routing length less than 500  
mils.



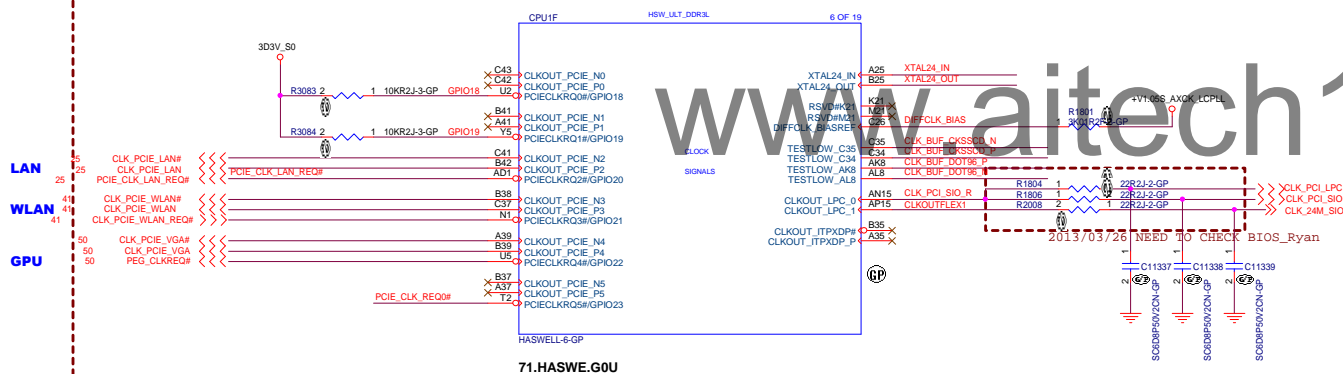
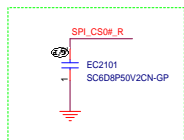
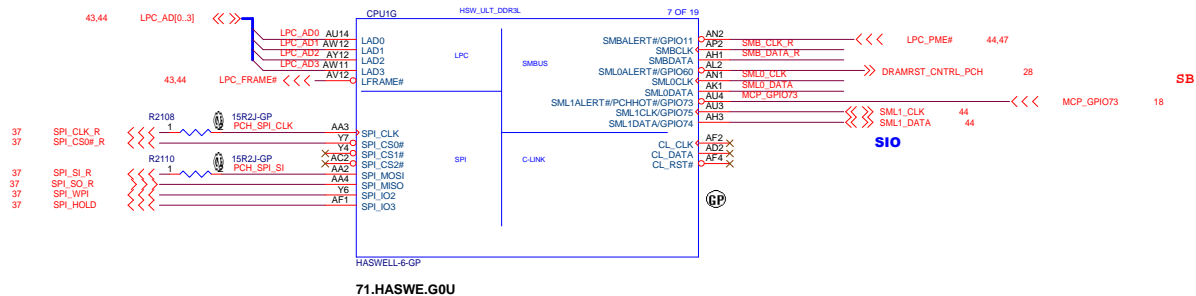
2013/04/25 delete Q1901 and relate components\_Ryan

2013/04/25 Merge components\_Ryan

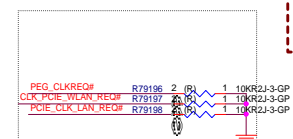
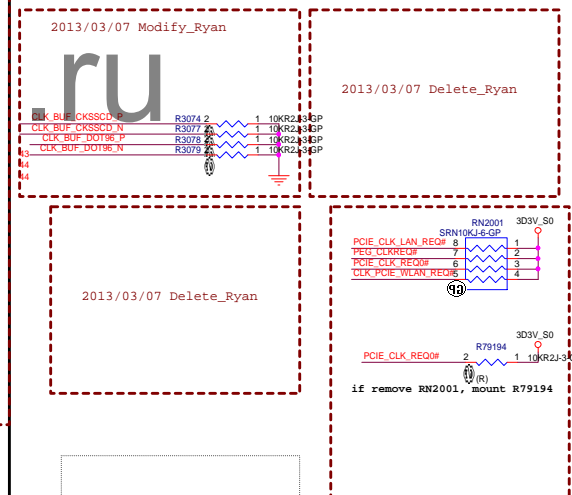
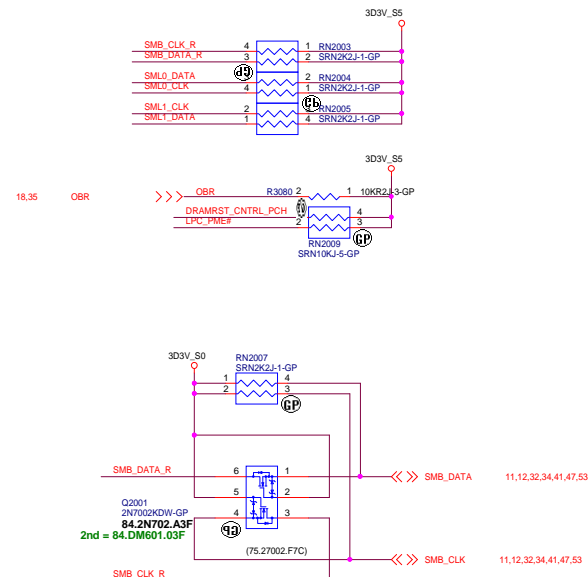
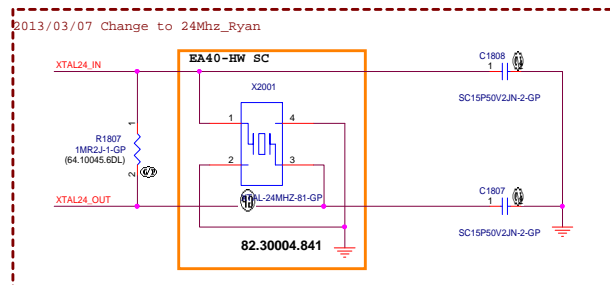




SSID = PCH



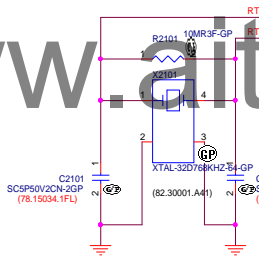
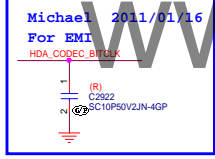
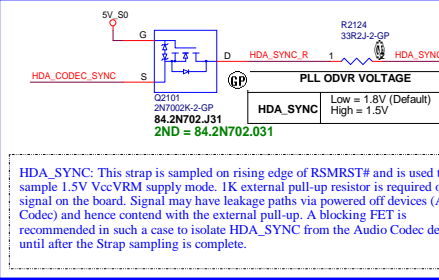
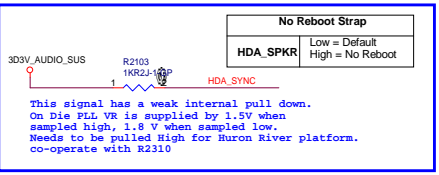
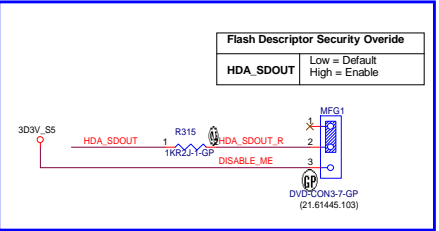
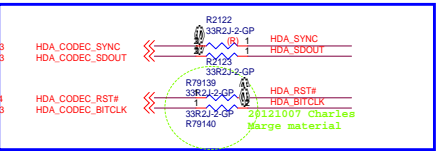
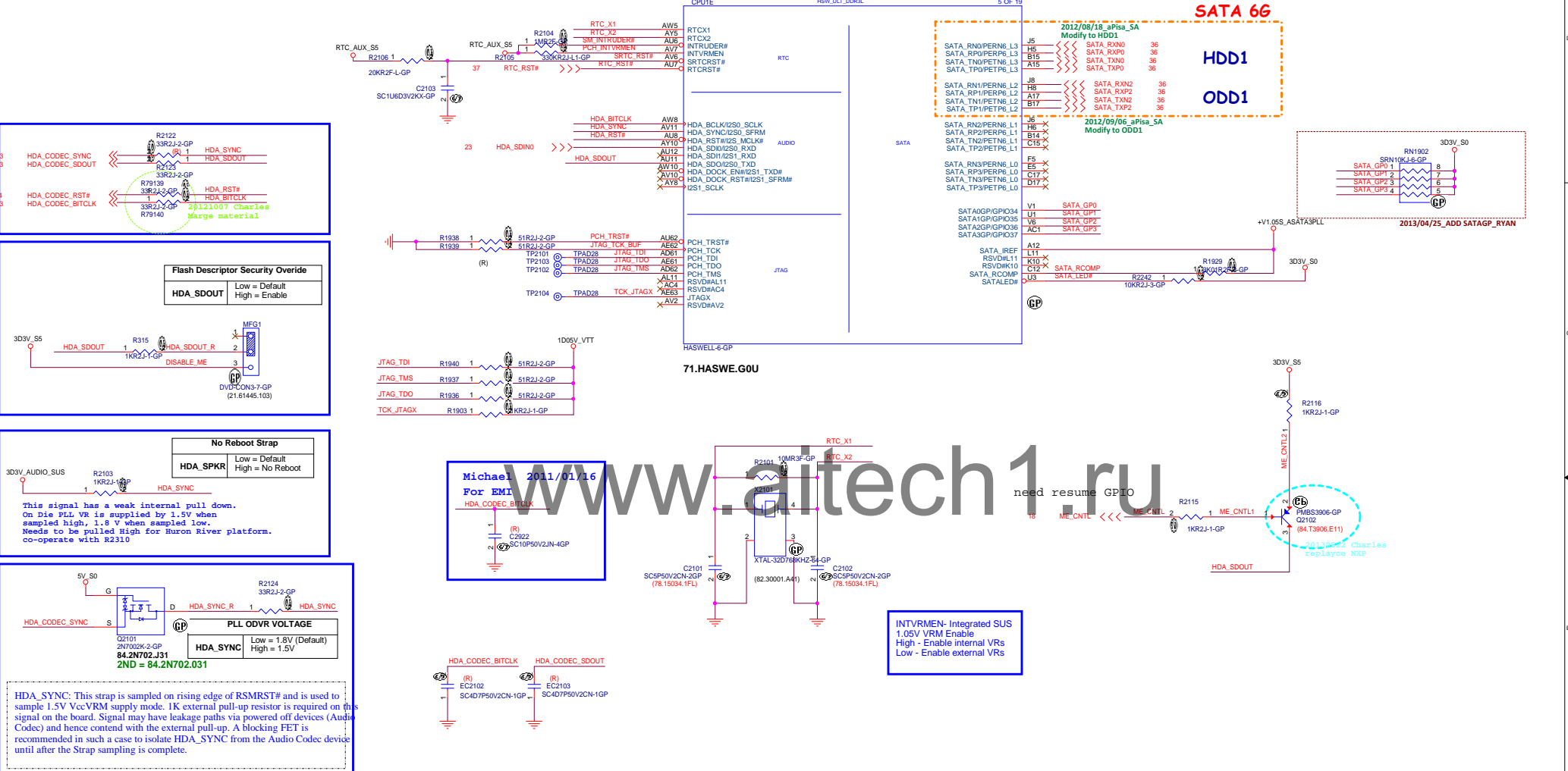
2013/03/04 CHANGE TO ONE CHIP\_Ryan



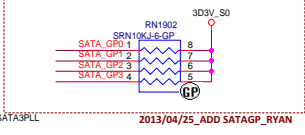
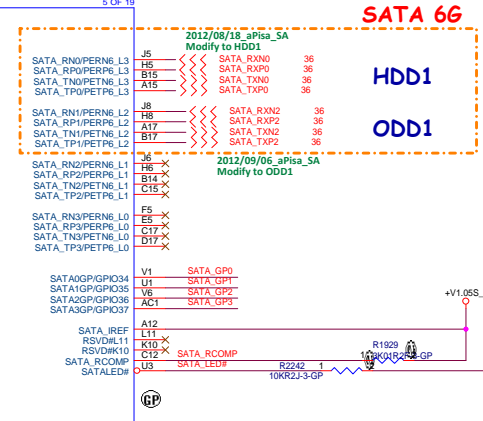
```
2013/07/22 pull low PCIE_CLK_LAN_REQ#,
CLK_PCIE_WLAN_REQ#, PEG_CLKREQ#
since don't support RTD3_RYAN
```



SSID = PCH



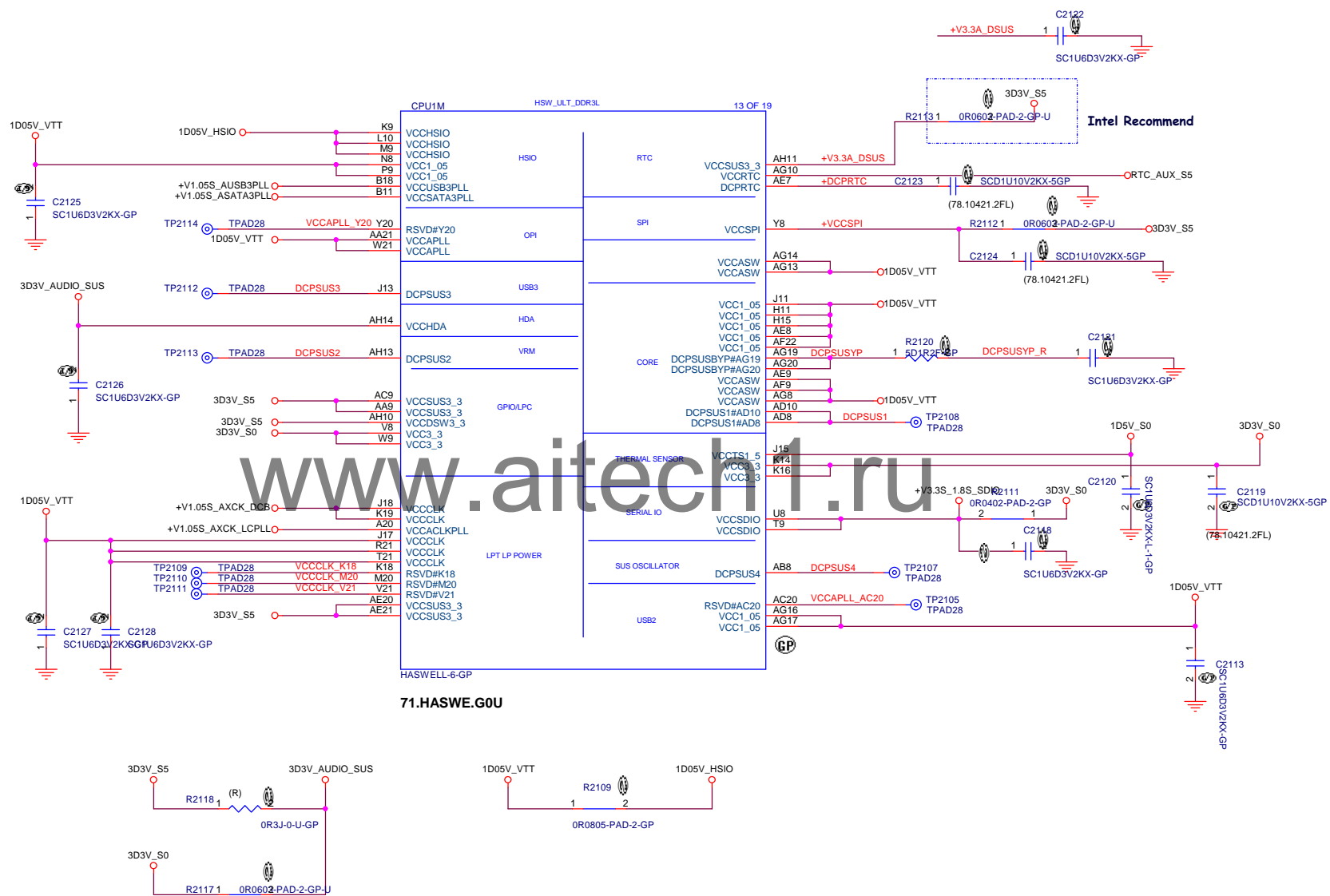
INTVRMEN- Integrated SUS  
1.05V VRM Enable  
High - Enable internal VRs  
Low - Enable external VRs





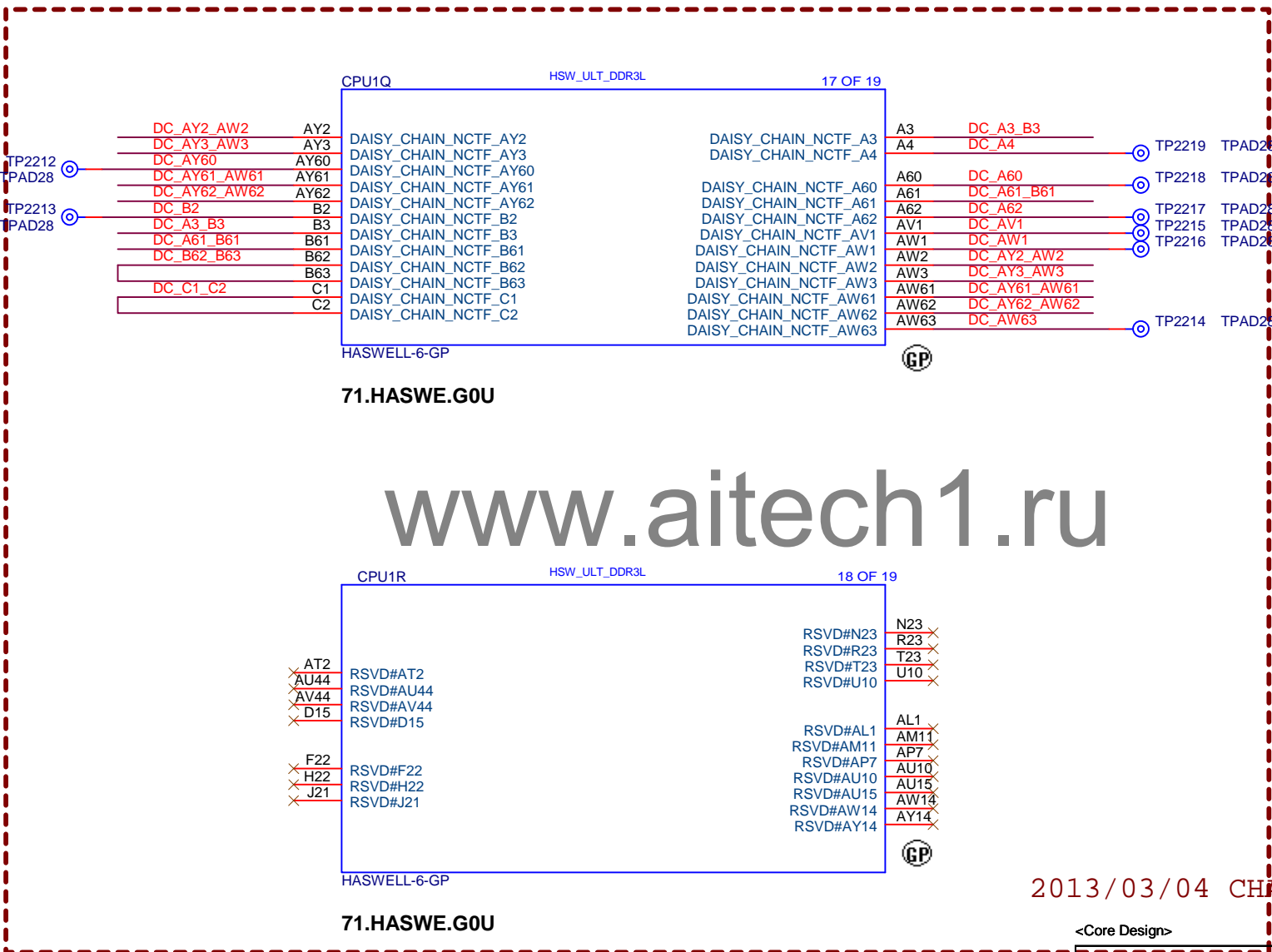






2013/03/18 CHANGE TO ONE CHIP\_Ryan  
<Core Design>





2013/03/04 CHANGE TO ONE CHIP\_Ryan

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**CPU ( RSVD )**

Size  
A4

Document Number

**aPISA2**

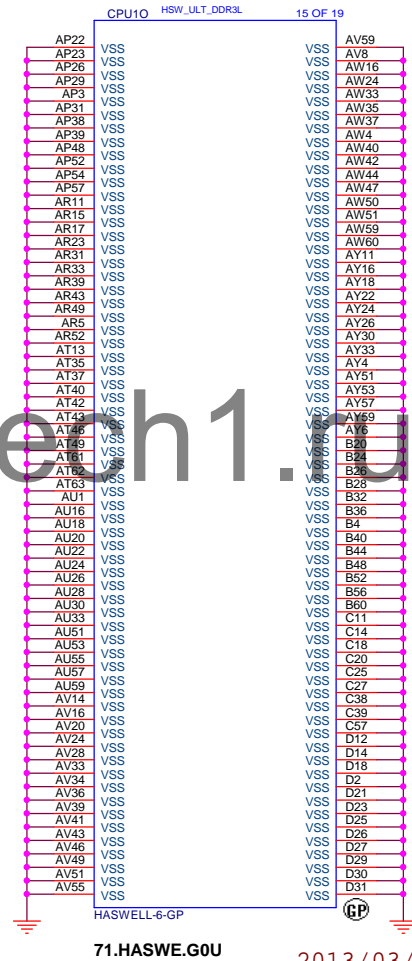
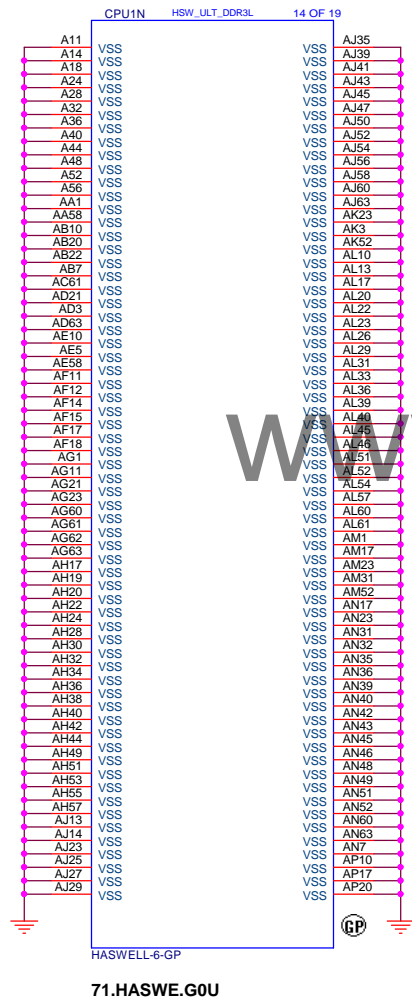
Rev  
**1A**

Date: Thursday, August 29, 2013

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SSID = PCH



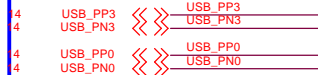
2013/03/04 CHANGE TO ONE CHIP\_Ryan



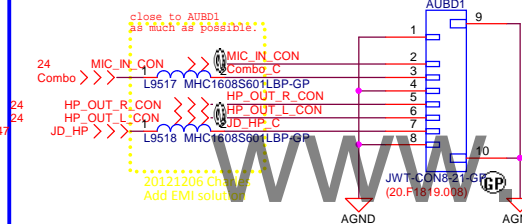
2012/09/04\_aPisa\_SA  
Delete USB3.0 Power

## USB3.0 CONNECTORFROM Co-lay

2012/08/18\_aPisa\_SA  
Delete USB3.0 Connector

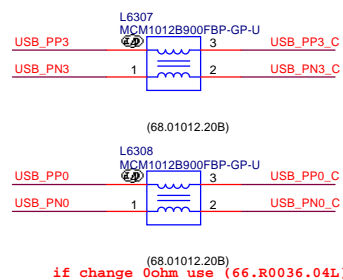


2012/08/24\_aPisa\_SA  
ADD AUBD1 connector

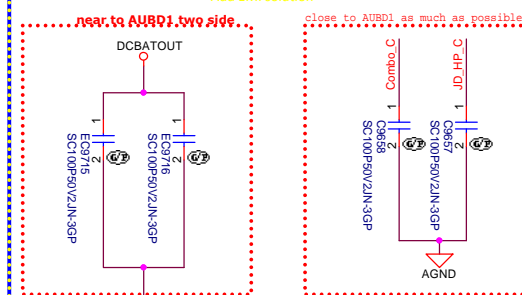


2012/09/10\_aPisa\_SA  
ADD EMC protect

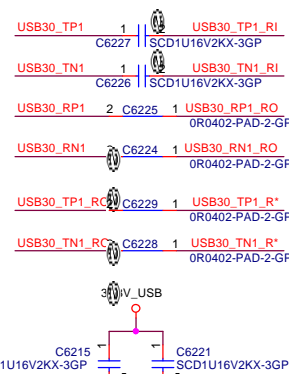
20121112 aPisa -1A Charles  
moune com-choke for card-reader USB2.0



20121205 Charles  
Add EMI solution



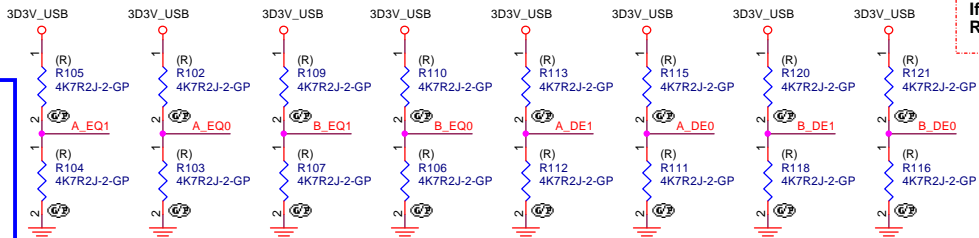
| Pin | Net         | Note     |
|-----|-------------|----------|
| 1   | Audio_GND   | GND      |
| 2   | MIC         | O analog |
| 3   | MIC_Verf    | O analog |
| 4   | Audio_GND   | GND      |
| 5   | Line out_R  | O analog |
| 6   | Line out_L  | O analog |
| 7   | Line out_JD | I        |
| 8   | Audio_GND   | GND      |



2012/07/10  
USB3.0 Redriver

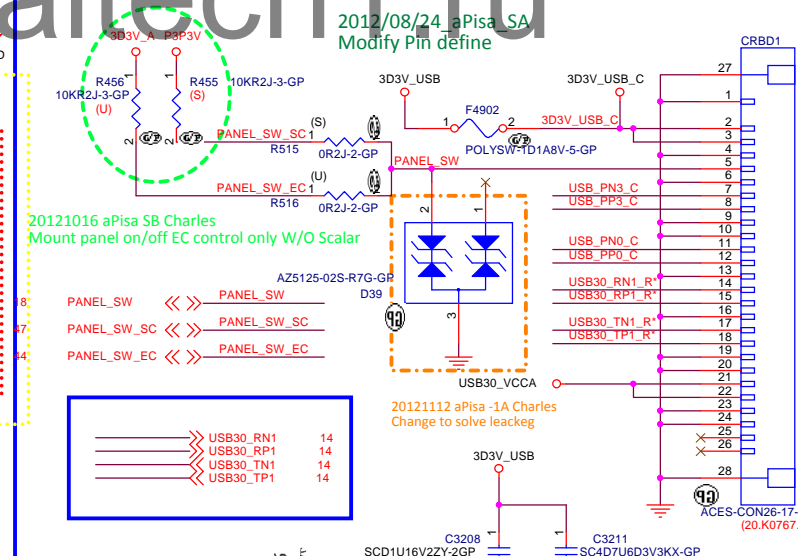
2012/07/12  
If use NXP  
R112,R118= 0ohm  
R80=NC

2012/07/12  
If use TI  
R112,R118,R80= 0ohm

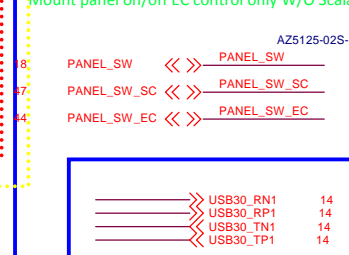


20121011 aPisa\_SA Charles  
Modify

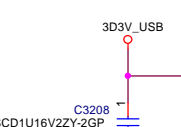
2012/08/24\_aPisa\_SA  
Modify Pin define



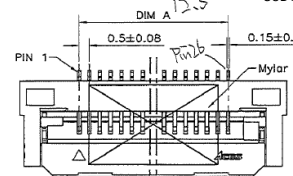
20121016 aPisa SA Charles  
Mount panel on/off EC control only W/O Scalar



20121112 aPisa -1A Charles  
Change to solve leakage



| Pin | Net           | Note             |
|-----|---------------|------------------|
| 1   | GND           | GND              |
| 2   | USB 3V        | I/O card reader  |
| 3   | USB 3V        | I/O card reader  |
| 4   | GND           | GND              |
| 5   | Switch        | I/O panel on/off |
| 6   | GND           | GND              |
| 7   | USB2.0 D+ #1  | I/O card reader  |
| 8   | USB2.0 D- #1  | I/O card reader  |
| 9   | GND           | GND              |
| 10  | GND           | GND              |
| 11  | USB3.0 TX+ #1 | I/O USB3.0       |
| 12  | USB3.0 TX- #1 | I/O USB3.0       |
| 13  | GND           | GND              |
| 14  | USB2.0 D+ #1  | I/O USB3.0       |
| 15  | USB2.0 D- #1  | I/O USB3.0       |
| 16  | GND           | GND              |
| 17  | USB3.0 RX+ #1 | I/O USB3.0       |
| 18  | USB3.0 RX- #1 | I/O USB3.0       |
| 19  | GND           | GND              |
| 20  | GND           | GND              |
| 21  | USB 5V        | I/O USB3.0       |
| 22  | USB 5V        | I/O USB3.0       |
| 23  | GND           | GND              |
| 24  | GND           | GND              |
| 25  | reserve       |                  |
| 26  | reserve       |                  |



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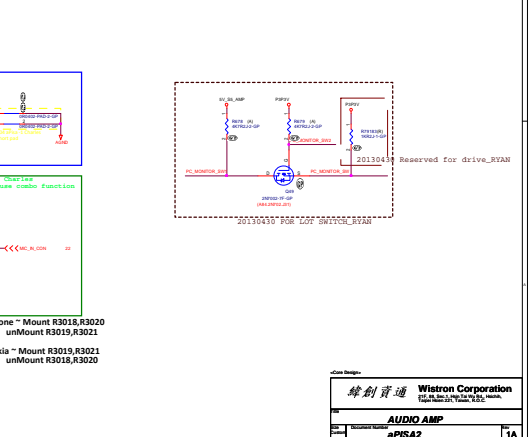
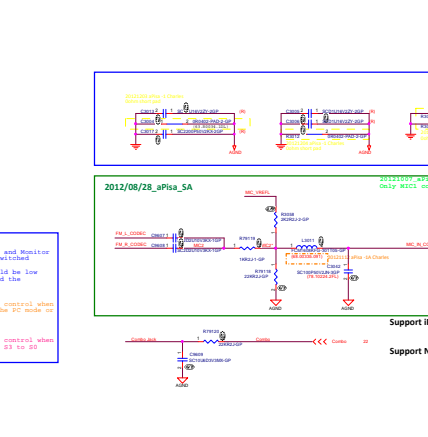
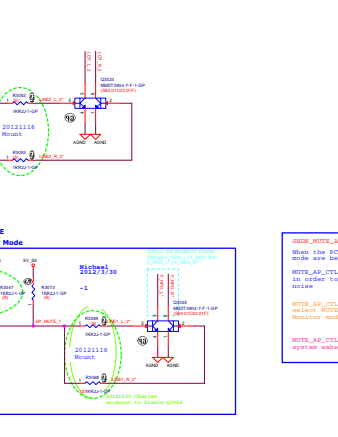
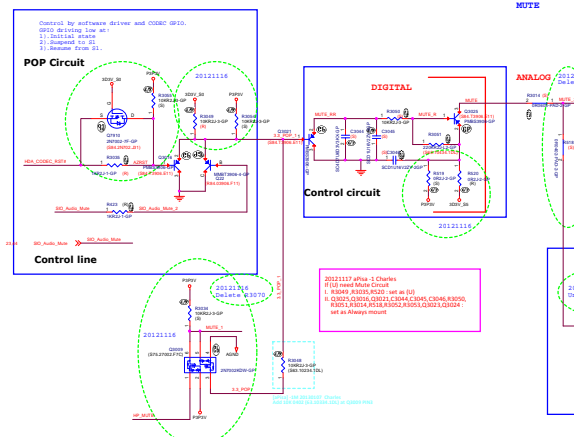
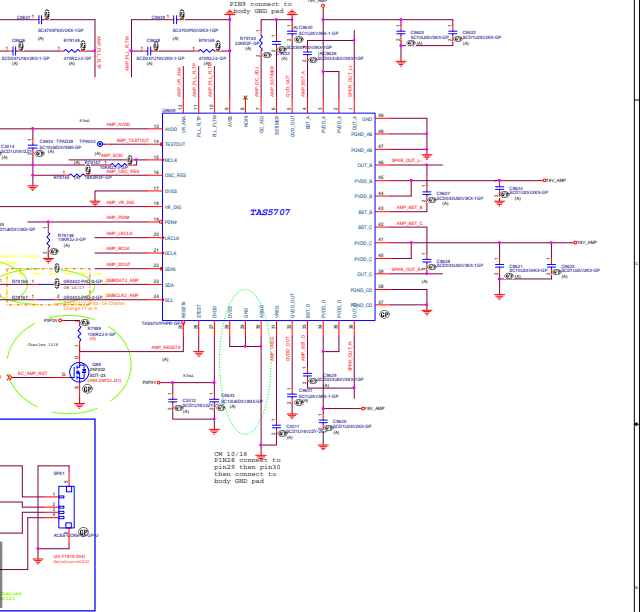
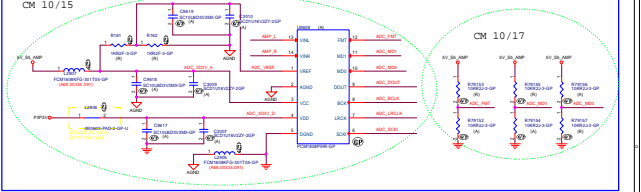
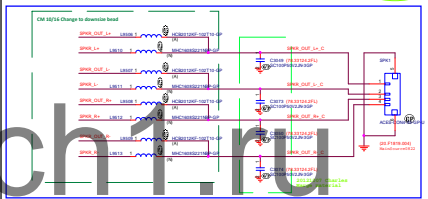
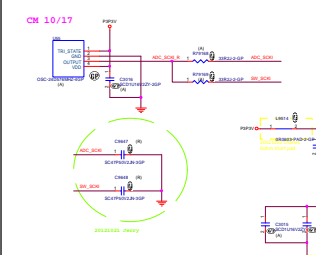
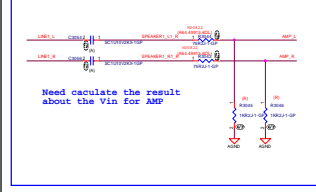
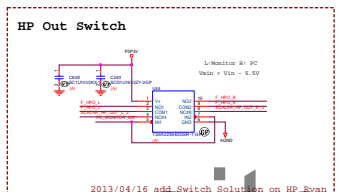
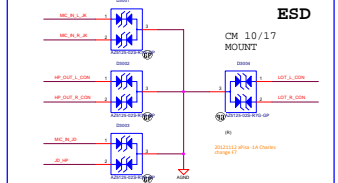
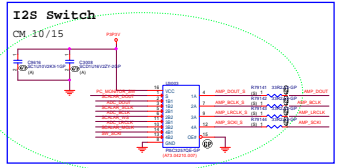
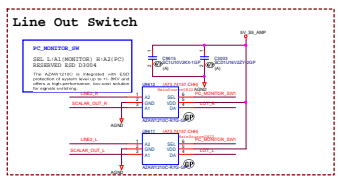
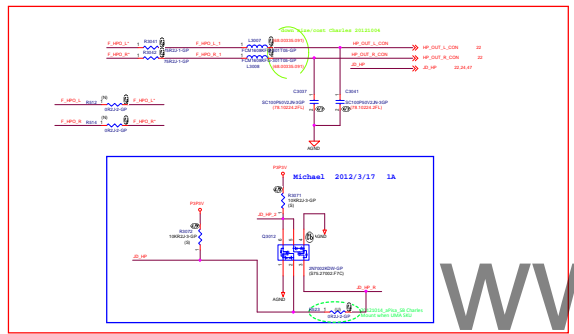
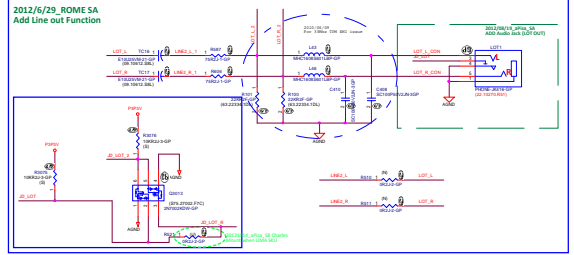
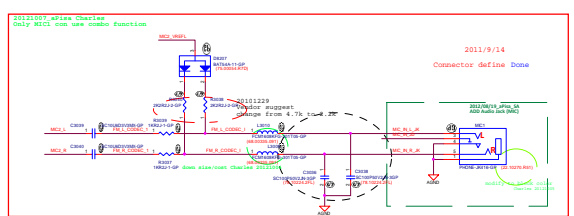
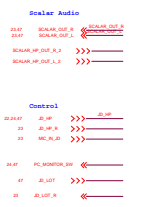
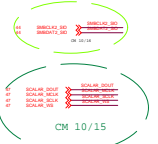
Front BD Connector  
aPISA2

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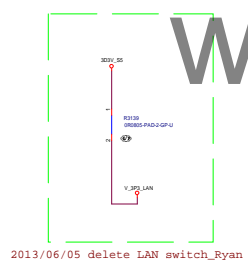
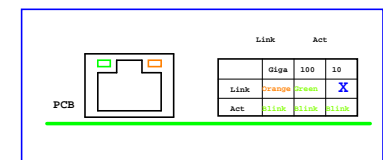
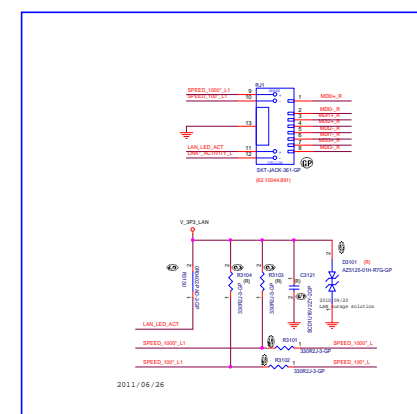
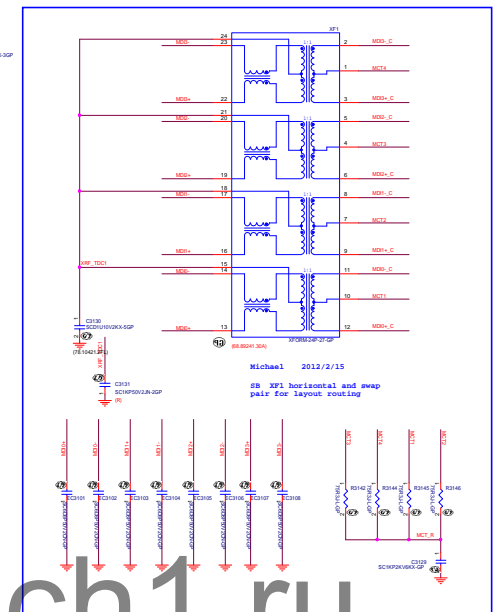
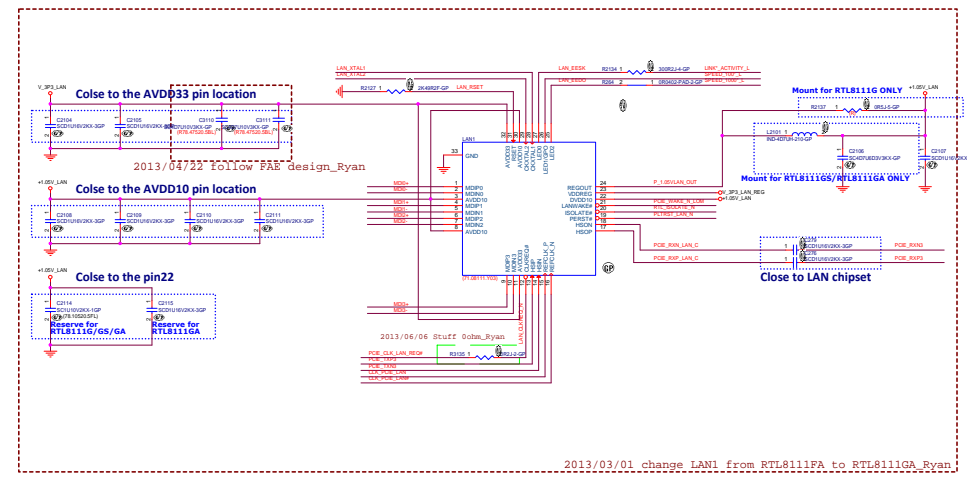
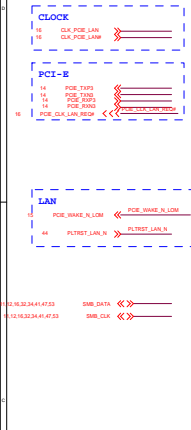




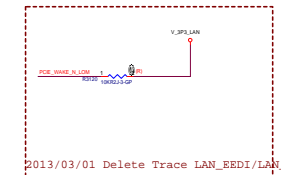
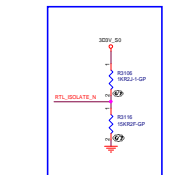
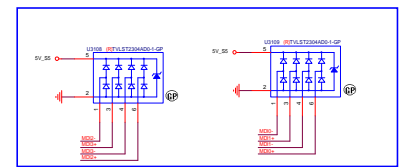
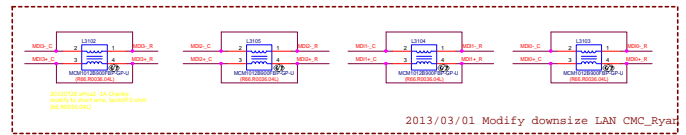
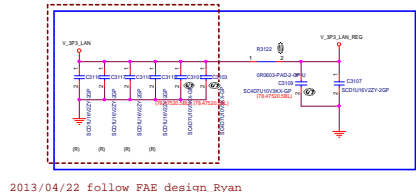
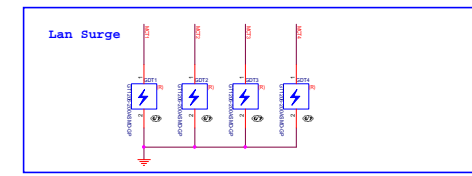








www.aitech1.ru





(SD, SDHC, MMC, MS, MS\_Pro, XD)

2012/07/12 Jerry  
Card reader move to small board

www.aitech1.ru

<Core Design>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**RTS5138 (CARD READER)**

Size  
Custom

Document Number

**aPISA2**

Rev

**1A**

Date: Thursday, August 29, 2013

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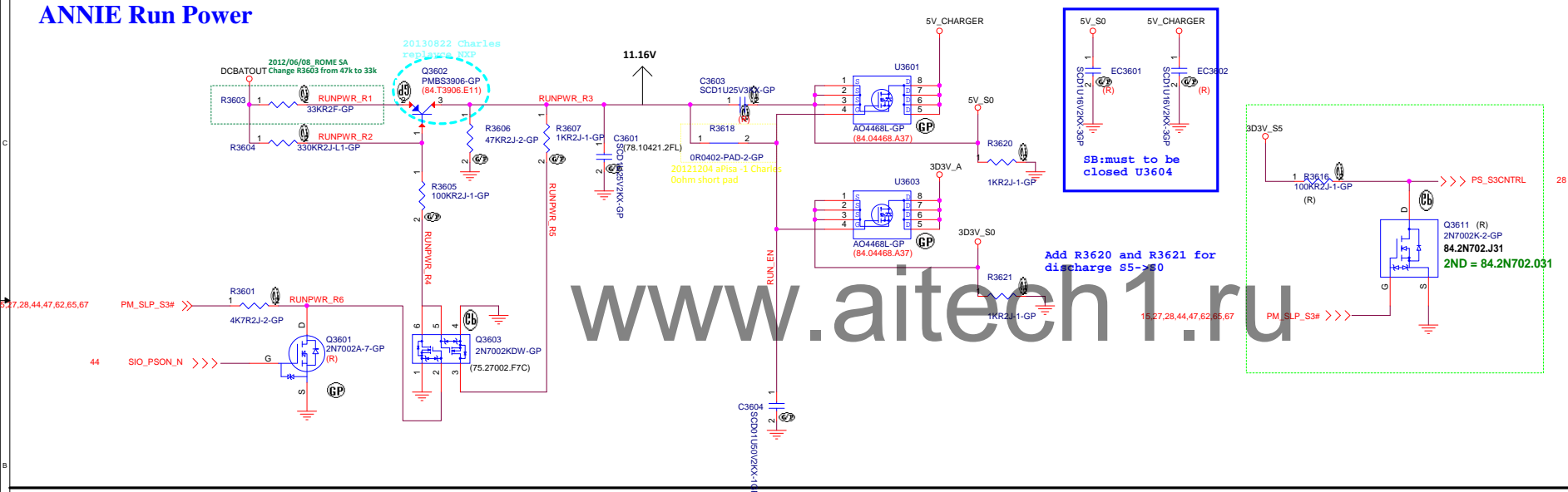
## Power Sequence

2013/06/26 Change time sequence for PCH\_PWRGD Ryan

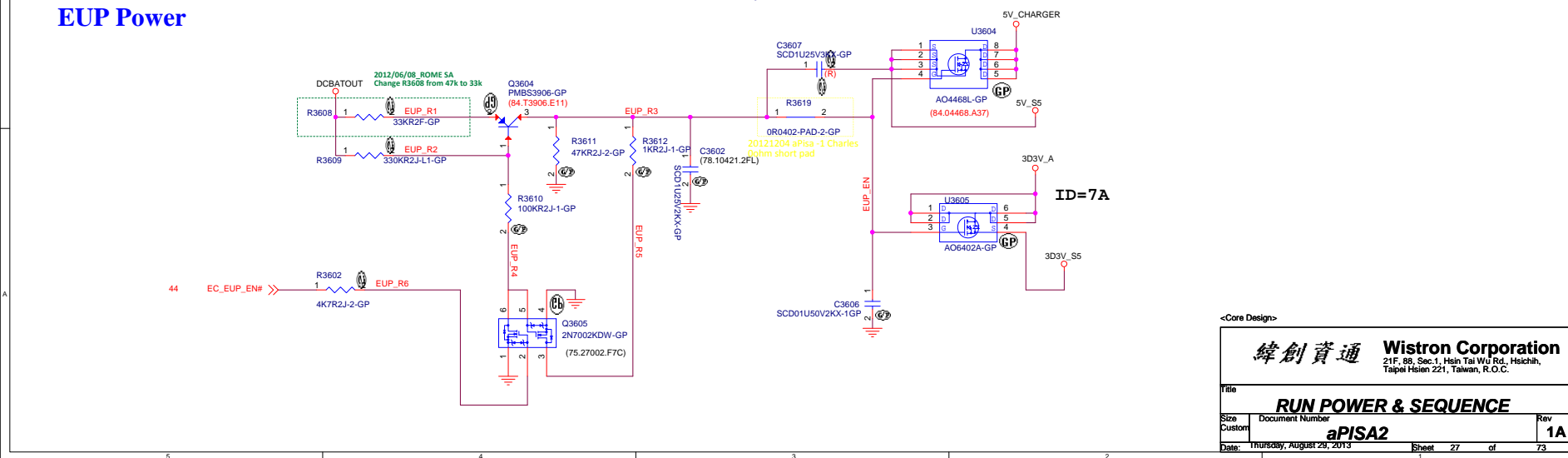


2011/9/22  
Reserve for  
system power  
ok

## ANNIE Run Power



## EUP Power





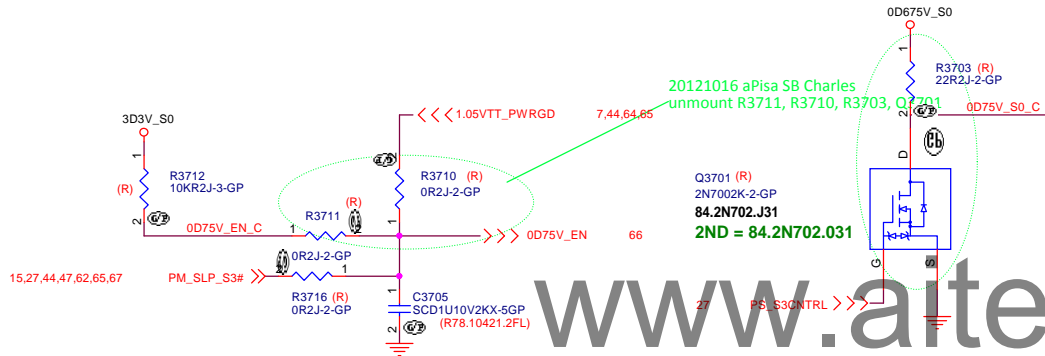
Close to CPU  
S3 Power Reduction Circuit Processor VREF\_DQ Implementation

20121012 Jerry  
Delete

5 S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

Close to DIMM  
S3 Power Reduction Circuit SM\_DRAMPWROK

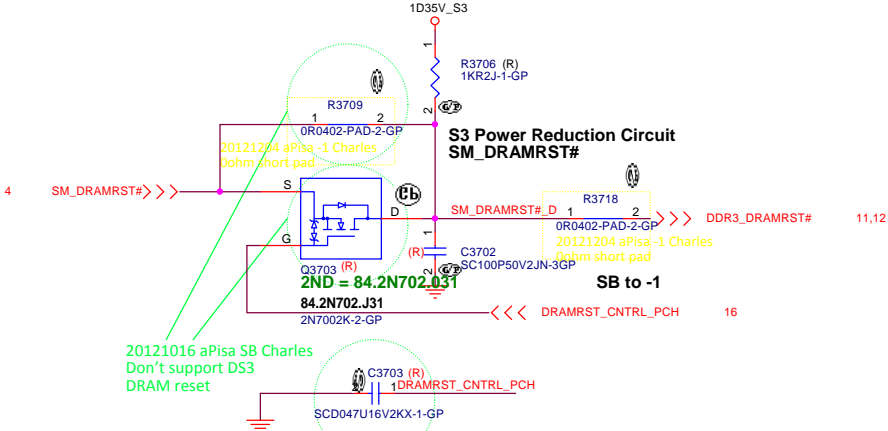
2013/03/11 Delete\_Ryan



www.aitech1.ru

2013/03/05 NO USED\_Ryan

Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK





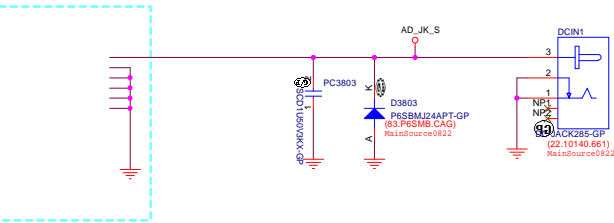
# ANNIE solution

Michael 2011/12/12

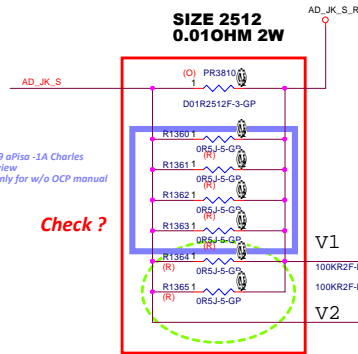
Remove Power connector about aNice  
Remain DC IN Jack

2011/9/19  
change AD+ to DCBATOUT  
20121016\_aPisa\_SB Charles  
Add F7 (O) for OCP solution

[aPisa] -1M 20130107 Charles  
Delete DCIN2



SIZE 2512  
0.010HM 2W

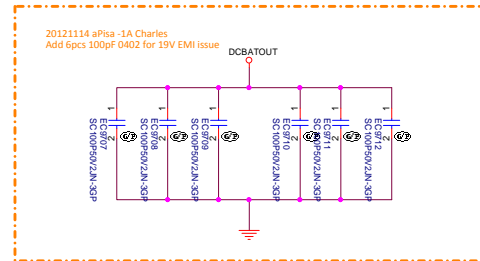
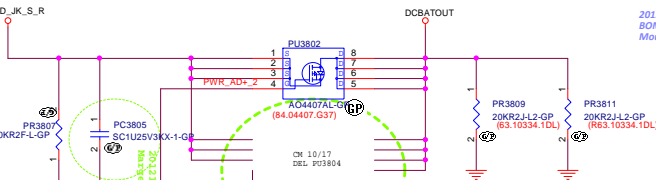


Check ?

20121119 aPisa -1A Charles  
BOM Review  
Mount Only for w/o OCP manual

Michael 2011/2/15

change the P/N of PU3802 and PU3804

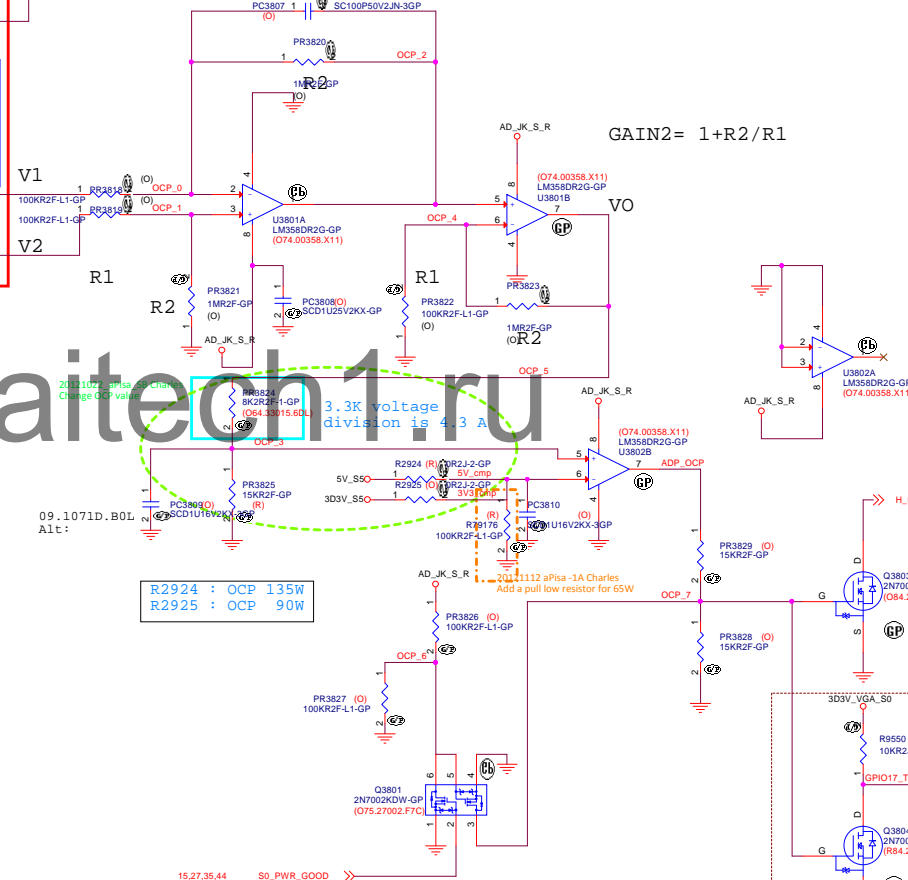


20121114 aPisa -1A Charles  
Add 6pcs 100pF 0402 for 19V EMI issue

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$$\text{GAIN1} = \text{VO} / (\text{V2} - \text{V1}) = \text{R2} / \text{R1}$$

$$\text{GAIN2} = 1 + \text{R2} / \text{R1}$$



R2924 : OCP 135W  
R2925 : OCP 90W

15.27.35.44 S0\_PWR\_GOOD

<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

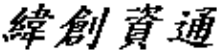
| Title     |                           |                |
|-----------|---------------------------|----------------|
| DCIN JACK |                           |                |
| Size      | Document Number           | Rev            |
| Custom    | aPISA2                    | 1A             |
| Date:     | Thursday, August 29, 2013 | Sheet 29 of 73 |



RESERVED

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<Core Design>

|                                                                                       |                 |                                                                                                             |           |
|---------------------------------------------------------------------------------------|-----------------|-------------------------------------------------------------------------------------------------------------|-----------|
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| Title                                                                                 |                 |                                                                                                             |           |
| <b>BATT CONN</b>                                                                      |                 |                                                                                                             |           |
| Size                                                                                  | Document Number |                                                                                                             | Rev       |
| A4                                                                                    | <b>aPISA2</b>   |                                                                                                             | <b>1A</b> |
| Date: Thursday, August 29, 2013                                                       |                 | Sheet 30 of                                                                                                 | 73        |



SSID = VIDEO

For UMA  
Low: Disable  
High: Enable

+19V\_S5\_INV Power

2013/03/07 change net name and co-layer\_Ryan

2013/03/28 change part\_Ryan  
F4901  
POLYSILOXANE24V-GP

Michael 2012/02/13  
add F4901 in SB

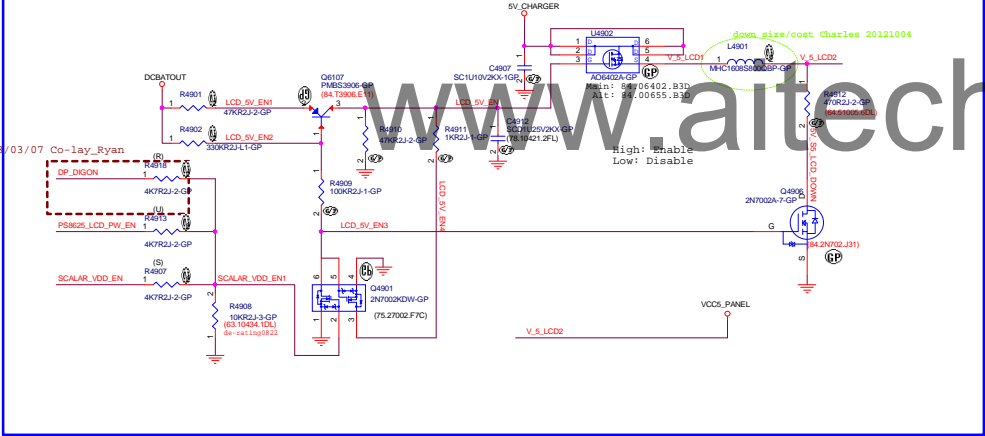
For SCALAR  
Low: Enable  
High: Disable

2013/03/07 change net name and co-layer\_Ryan

LVDS For SCALAR



2013/03/07 Co-layer\_Ryan



LVDS For PCH

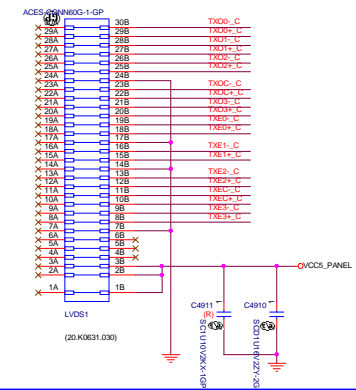


2013/03/06 change LVDS net name of transmitter\_Ryan



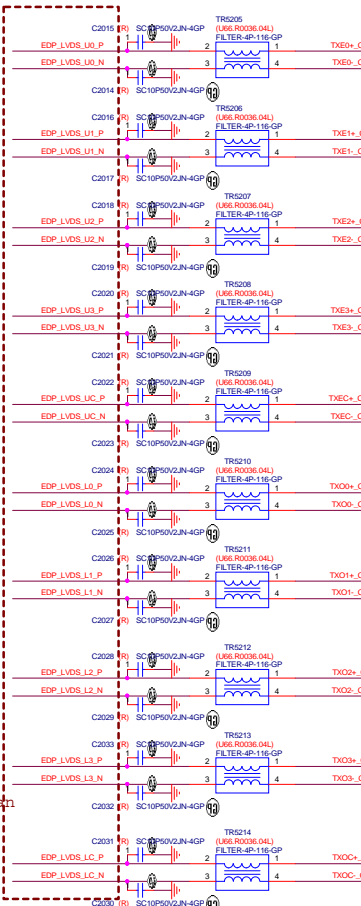
2012/06/22 SA

Change LVDS connector



20121014 aPisa SB Charles  
Add comm-mode choke, EMC Cap  
for PCH to LVDS

20121112 aPisa -1A Charles  
Add F7-U to mount only when 70 SKU

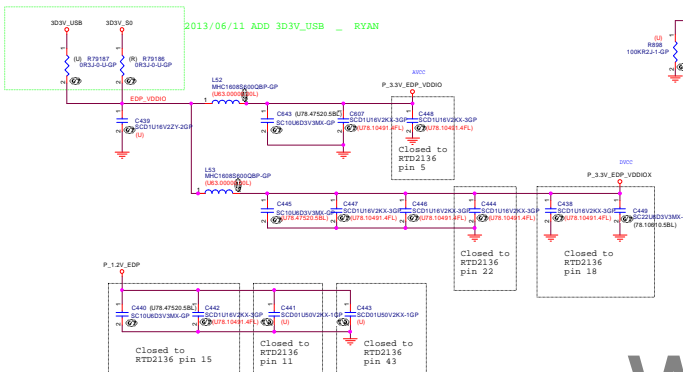
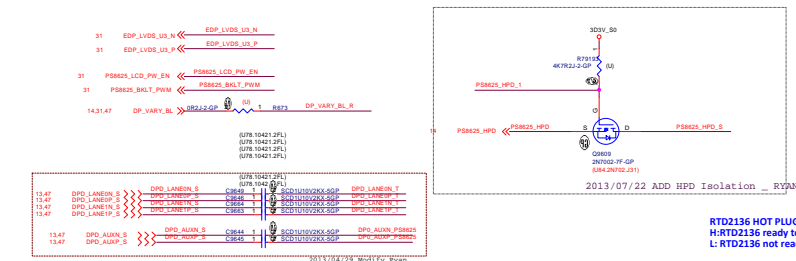


2013/04/24 place as close as CMC TR5205~TR5214\_Ryan

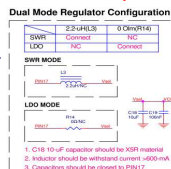
2013/03/06 change LVDS net name of transmitter\_Ryan



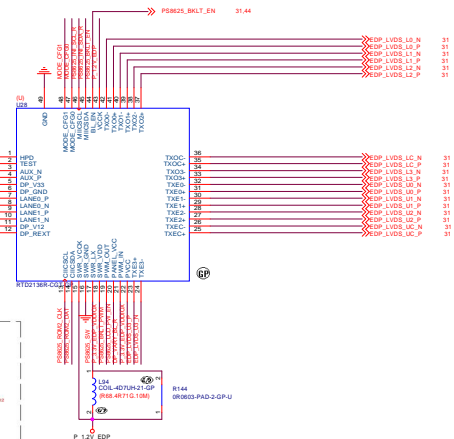
# SSID = VIDEO HDMI Level Shifter & CONNECTOR



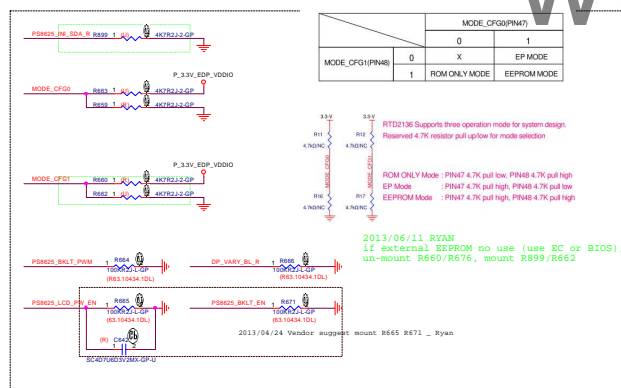
RTD2136 HOT PLUG  
H:RTD2136 ready to take input  
L: RTD2136 not ready



2013/03/06 add U28 RTD2136 eDP to LVDS transmitter(Dallas)\_Ryan



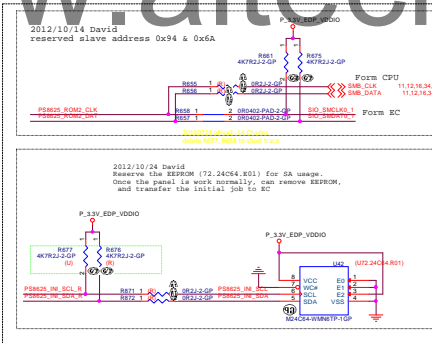
www.aitech1.ru



| MODE_CFG(PIN#7) |   |               |
|-----------------|---|---------------|
| MODE_CFG(PIN#8) | 0 | 1             |
|                 | X | EP MODE       |
|                 | 1 | ROM ONLY MODE |

RTD2136 Supports three operation mode for system design.  
Reserved 4.7K resistor pull up for mode selection.

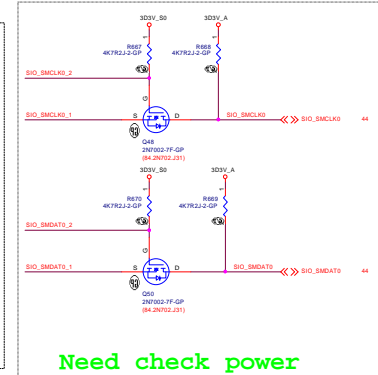
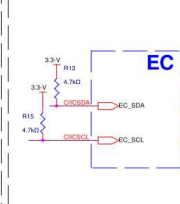
ROM ONLY Mode : PIN#7 4.7K pull low, PIN#8 4.7K pull high  
EP Mode : PIN#7 4.7K pull high, PIN#8 4.7K pull low  
EEPROM Mode : PIN#7 4.7K pull high, PIN#8 4.7K pull high



EEPROM Mode  
In EEPROM mode, an additional EEPROM is needed.  
EEPROM should configure with following condition.

- 1- EEPROM with a size 8K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8

EP Mode  
External device connect to DP2LVDS by  
Pin13/Pin14, I2C protocol is used

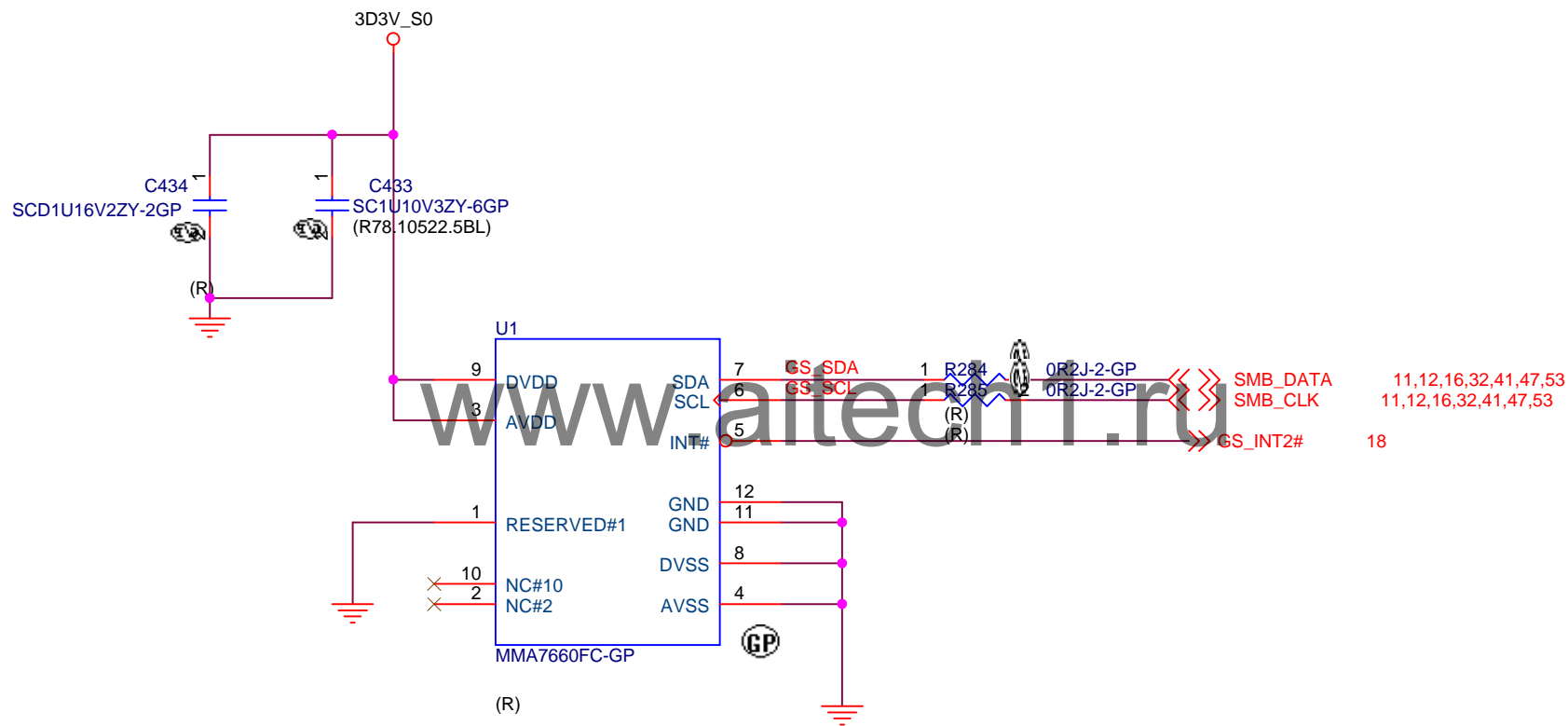








# G-Sensor



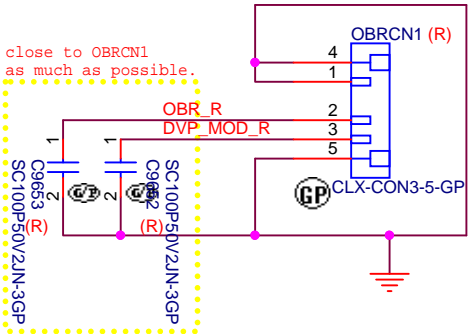
<Core Design>

|                                                                                                                                                   |                           |
|---------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|
| <div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> </div> |                           |
| Title                                                                                                                                             |                           |
| G-SENSOR                                                                                                                                          |                           |
| Size                                                                                                                                              | Document Number           |
| A                                                                                                                                                 | aPISA2                    |
| Date:                                                                                                                                             | Thursday, August 29, 2013 |
| Sheet                                                                                                                                             | 34 of 73                  |
| Rev                                                                                                                                               | 1A                        |

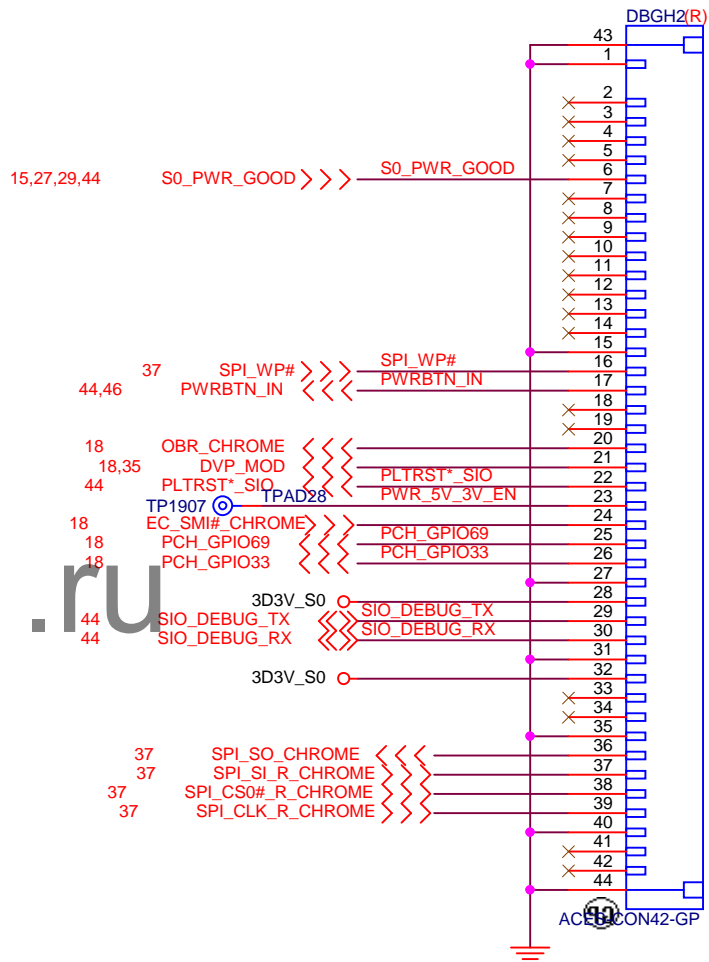
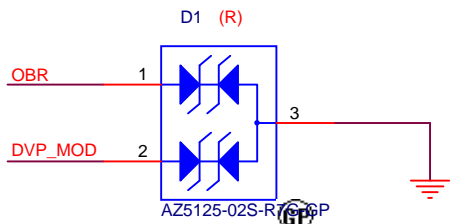
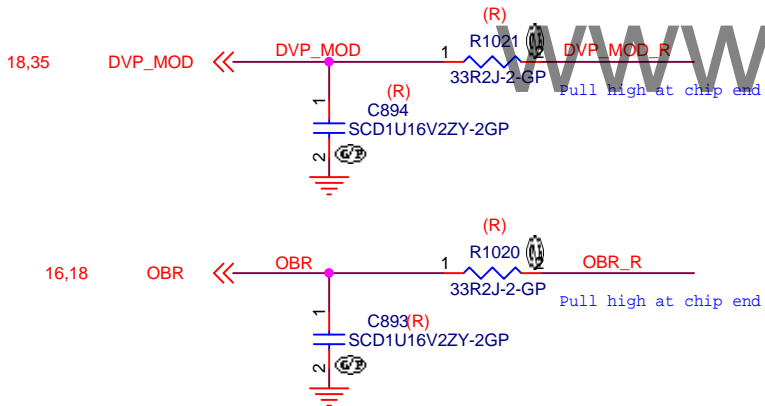


# Chrome OBR Fun

2012/09/07\_aPisa\_SA  
Add OBR Button



20121205 Charles  
Add EMI solution



<Core Design>

|                                       |                                  |                                                                               |                  |
|---------------------------------------|----------------------------------|-------------------------------------------------------------------------------|------------------|
| <b>緯創資通</b>                           |                                  | <b>Wistron Corporation</b>                                                    |                  |
|                                       |                                  | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                  |
| Title                                 |                                  |                                                                               |                  |
| <b>ChromeOS OBR / Debug connector</b> |                                  |                                                                               |                  |
| Size<br>A4                            | Document Number<br><b>aPISA2</b> |                                                                               | Rev<br><b>1A</b> |
| Date:                                 | Thursday, August 29, 2013        | Sheet 35 of                                                                   | 73               |

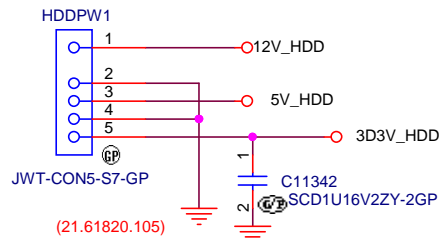
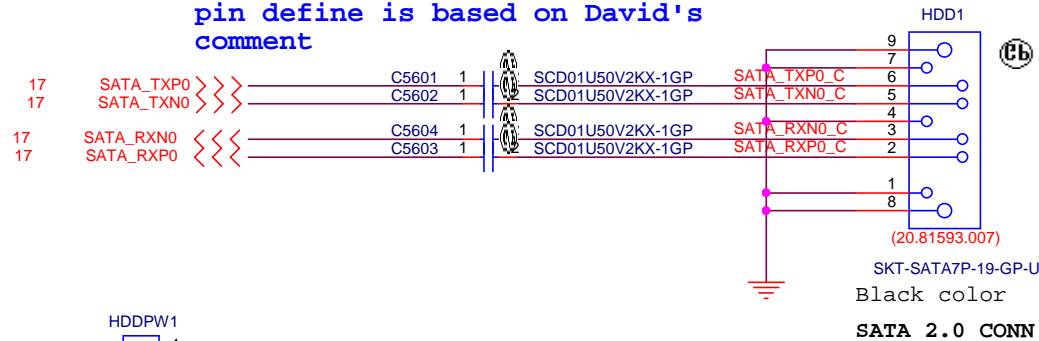


SSID = SATA

# SATA HDD Connector

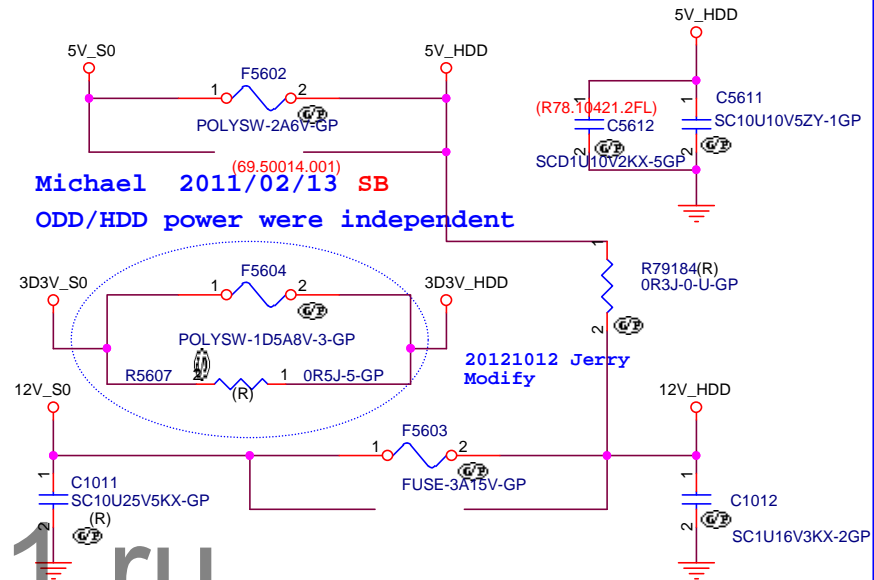
Michael 2012/01/03

pin define is based on David's comment



2013/06/24\_CLOSE HDDPW1\_EMI

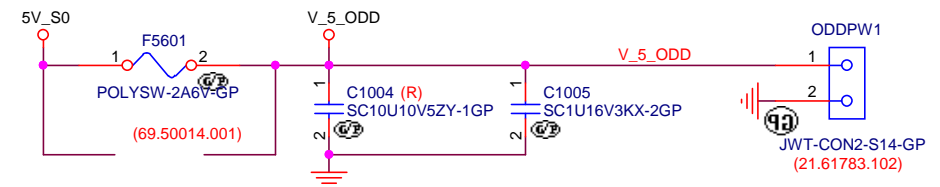
Layout: Put them together



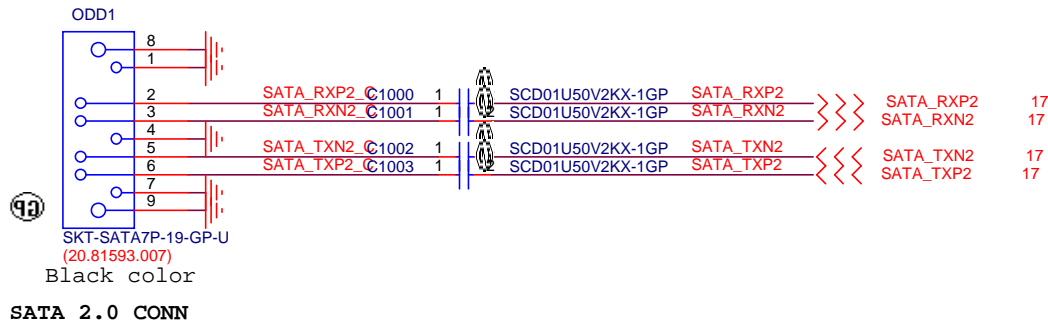
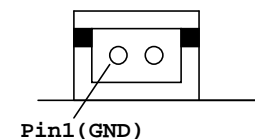
Michael 2011/02/13 SB  
ODD/HDD power were independent

20121012 Jerry Modify

## ODD SATA POWER CONNECTOR



Front View



2012/08/18\_aPisa\_SA  
ADD ODD

20.60341.104: 4pin right angle  
20.60334.103: 3pin right angle

<Core Design>

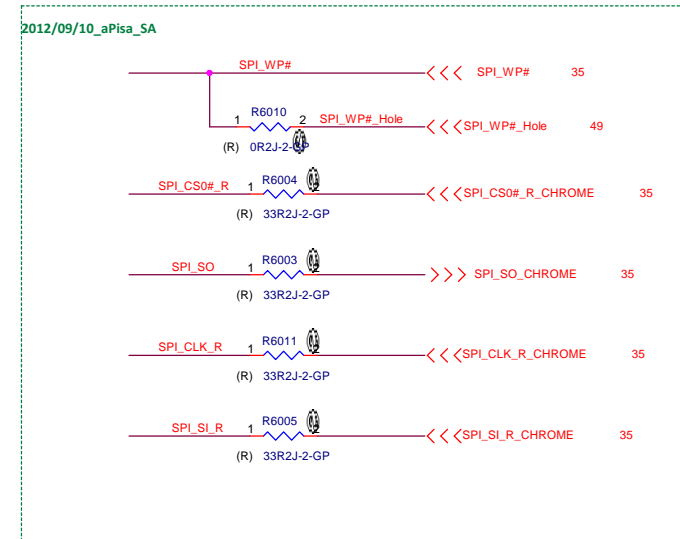
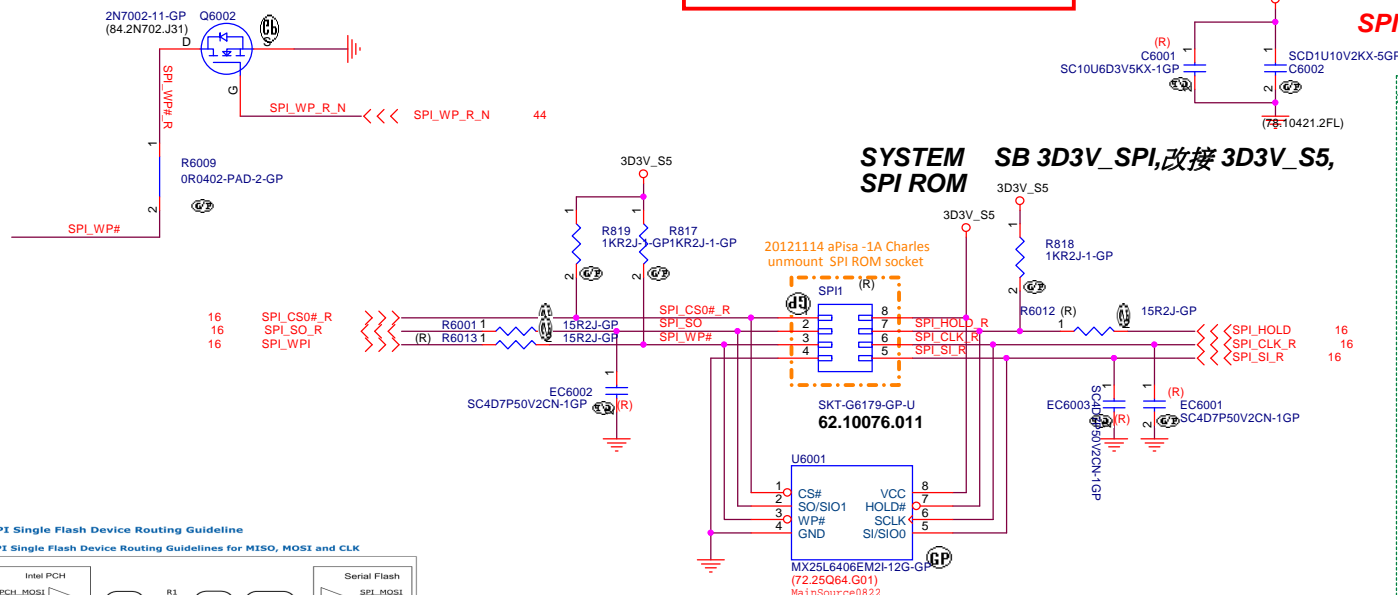
|                                                                            |                           |                |
|----------------------------------------------------------------------------|---------------------------|----------------|
| 緯創資通 Wistron Corporation                                                   |                           |                |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |                           |                |
| Title                                                                      |                           |                |
| HDD/ODD                                                                    |                           |                |
| Size                                                                       | Document Number           | Rev            |
| Custom                                                                     | aPISA2                    | 1A             |
| Date:                                                                      | Thursday, August 29, 2013 | Sheet 36 of 73 |



```
SSID = Flash.ROM
```

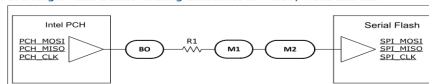
**SPI ROM Equal length need to less than 500mil**

**SPI ROM Equal length need to less than 500mil**

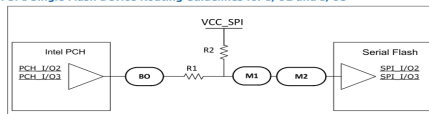


#### 22.3.1.1 SPI Single Flash Device Routing Guideline

**Figure 22-2. SPI Single Flash Device Routing Guidelines for MISO, MOSI and CLK**



**Figure 22-3. SPI Single Flash Device Routing Guidelines for I/O2 and I/O3**



**Note:** I/O2 and I/O3 connection has to be pulled up with 1k ohm

**Figure 22-4. SPI Single Flash Device Routing Guidelines for CS0#**

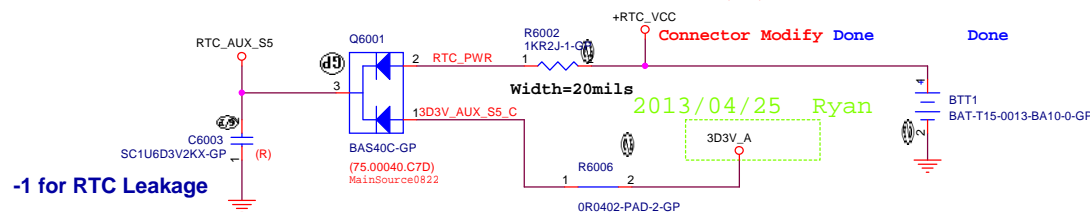


**Table 22-3. SPI Single Flash Device Routing Guidelines (Sheet 2 of 2)**

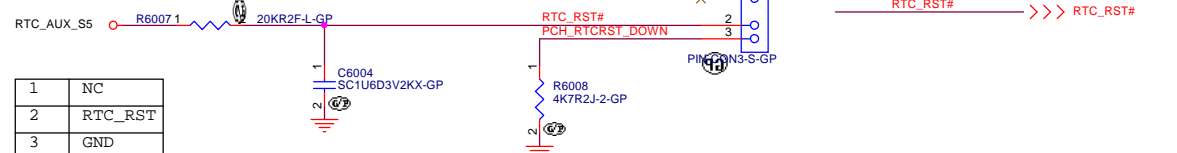
| Parameter             | Segment    | Stackup | Unit | Routing Recommendation |
|-----------------------|------------|---------|------|------------------------|
| Breakout Trace Length | BO         | MS,SL   | inch | < 1"                   |
| Length 1              | M1         | MS,SL   | inch | 1" - 5"                |
| Length 2              | M2         | MS,SL   | inch | 0.5" - 1"              |
| Total length          | BO, M1, M2 | MS,SL   | inch | 1.5" - 7"              |
| Resistor              | R1         |         | ohm  | 15                     |
| Resistor              | R2         |         | ohm  | 1k                     |

2012/01/03

**SSID = RBATT**



## Clear CMOS



2011/9/30

## Add CLR CMOS circuit

**<Core Design>**

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Taipei Hsien 221, Taiwan, R.O.C.

| Title |
|-------|
|-------|

**SPI/RTC**

Size

|  |                 |
|--|-----------------|
|  | Document Number |
|--|-----------------|

**aPISA2**

Rev

Date: Thursday, August 29, 2013

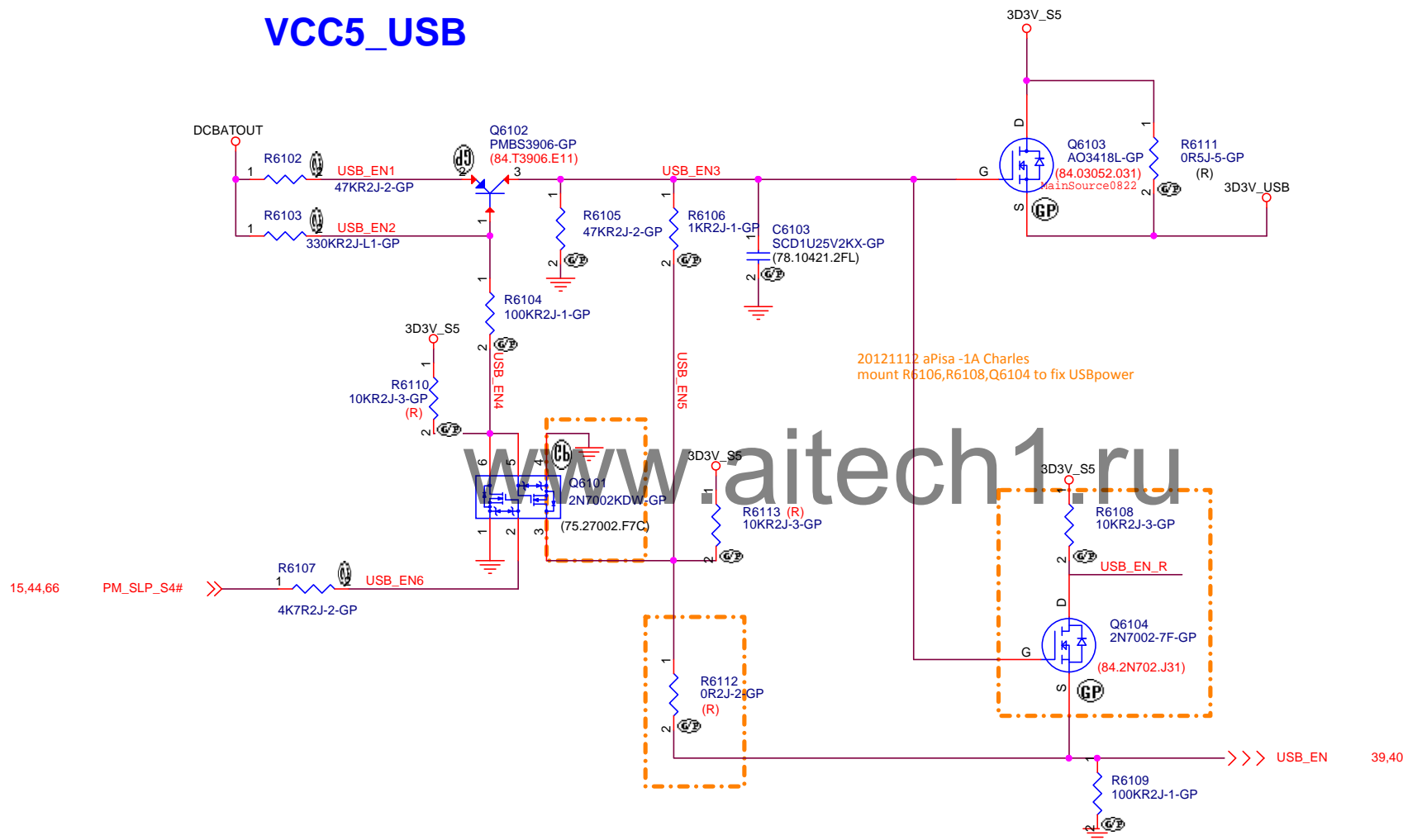
Sheet 3

73



SSID = USB

VCC5\_USB



<Core Design>

緯創資通

**Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**USB2.0 Power SW**

Size  
Custom

Document Number

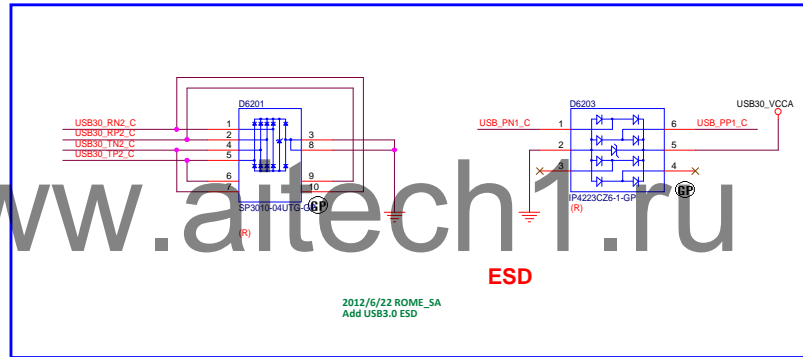
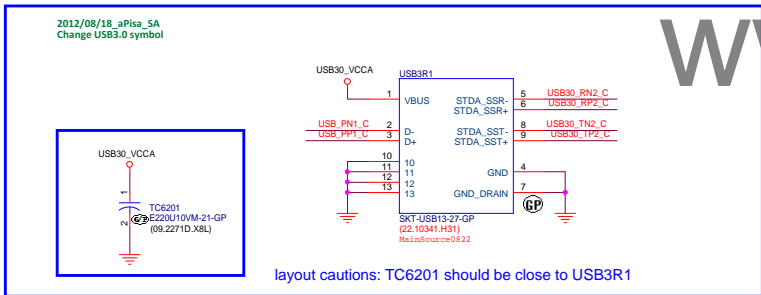
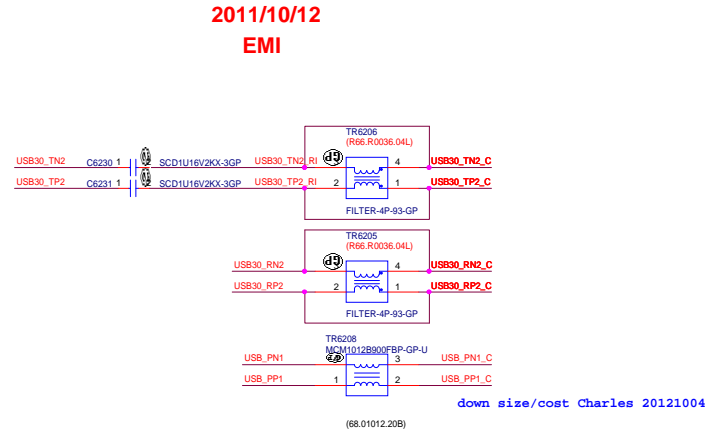
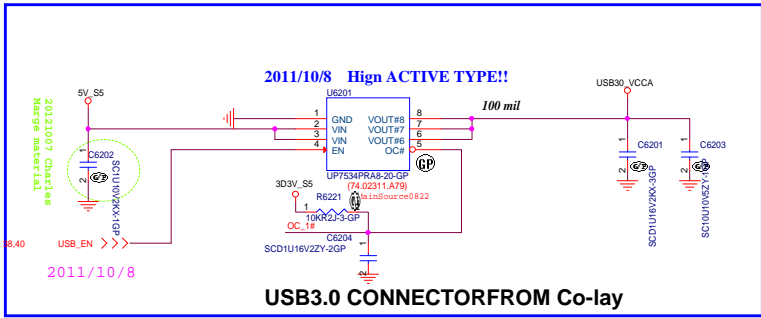
**aPISA2**

Rev  
**1A**

Date: Thursday, August 29, 2013

Sheet 38 of 73





| USB 3.0 Connector Pin definition |                          |
|----------------------------------|--------------------------|
| 1                                | POWER                    |
| 2                                | USB 2.0 D-               |
| 3                                | USB 2.0 D+               |
| 4                                | GND                      |
| 5                                | StdA_SSRX- SuperSpeed RX |
| 6                                | StdA_SSRX+               |
| 7                                | GND                      |
| 8                                | StdA_SSTX- SuperSpeed TX |
| 9                                | StdA_SSTX+               |

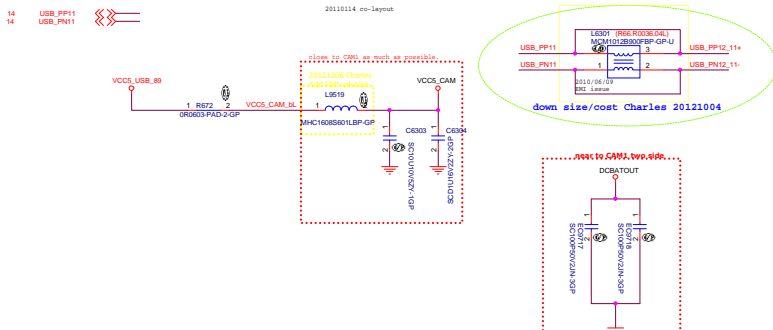


```
SSID =USB2.0
```

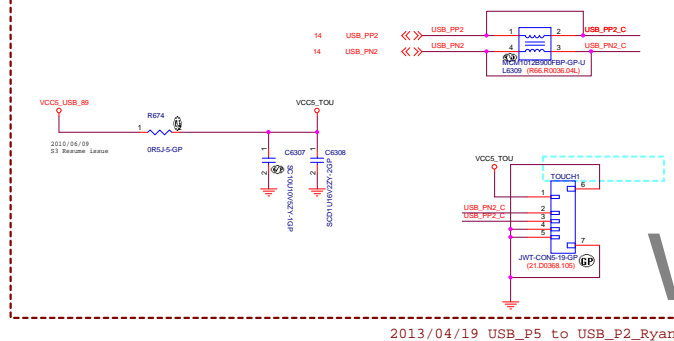
USB Port11 -> WEB CAM

2011/10/18

20110114\_co-layout

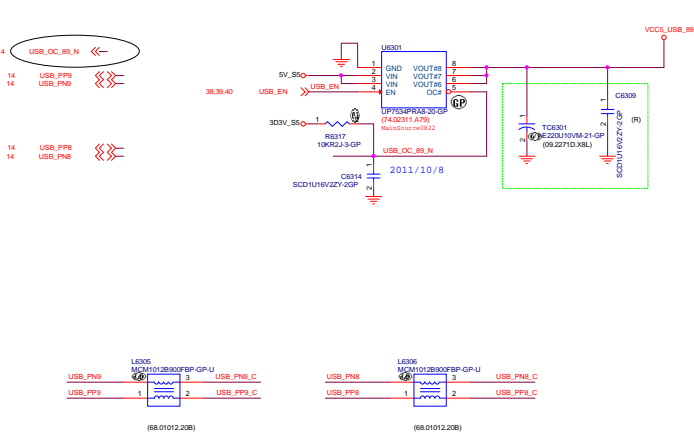


USB Port 2 -> TOUCH

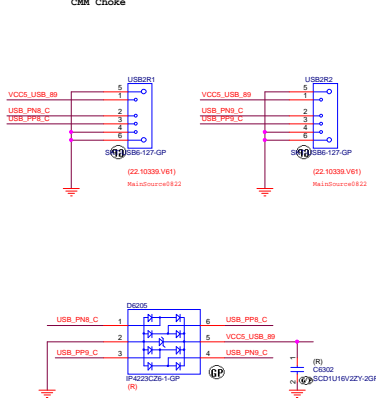


2013/04/19 USB\_P5 to USB\_P2\_Ryan

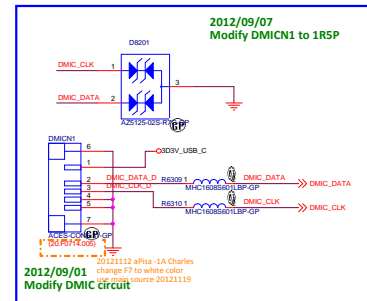
USB Port 8,9-> REAR I/O



Reserve EMI  
CMM Choke

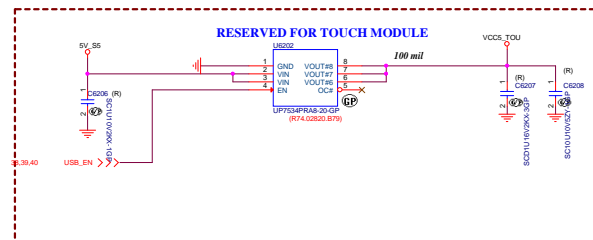


*DMIC Connector*



2012/06/29 Jerry  
Delete IR Function

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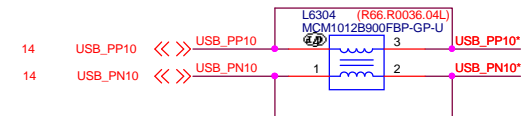



### *Mini Card Connector(Wireless LAN+BT)*

Michael  
ADD USB for BT Function

Height: 5.2mm  
T-CONN: 62.10043.831  
BELLWETHER: 62.10043.A81

Michael 2011/11/29  
Change 3D3V\_S0 to 3D3V\_EUP




|                                                                                       |                           |                                                                                                             |          |
|---------------------------------------------------------------------------------------|---------------------------|-------------------------------------------------------------------------------------------------------------|----------|
| <Core Design>                                                                         |                           |                                                                                                             |          |
|  |                           | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |          |
| Title                                                                                 |                           |                                                                                                             |          |
| <b>Mini PCIE Card WLAN / BT</b>                                                       |                           |                                                                                                             |          |
| Size                                                                                  | Document Number           | Rev                                                                                                         |          |
| Custom                                                                                |                           | 1A                                                                                                          |          |
| <b>aPISA2</b>                                                                         |                           |                                                                                                             |          |
| Date                                                                                  | Thursday, August 29, 2013 | Sheet                                                                                                       | 41 of 73 |



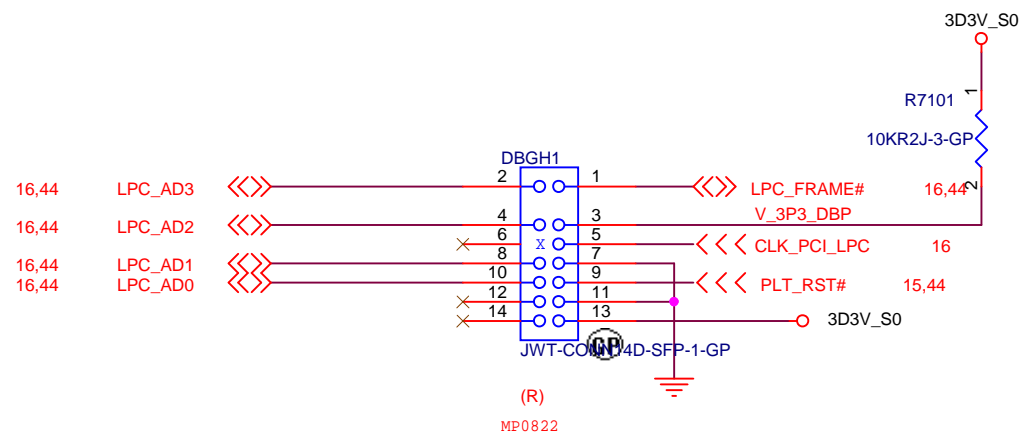
2012/08/18\_aPisa\_SA  
Delete mSATA

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<Core Design>

|                                                                                       |                                  |                                                                                                             |                  |
|---------------------------------------------------------------------------------------|----------------------------------|-------------------------------------------------------------------------------------------------------------|------------------|
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| Title                                                                                 |                                  |                                                                                                             |                  |
| <b>Mini PCIE Card mSATA</b>                                                           |                                  |                                                                                                             |                  |
| Size<br>Custom                                                                        | Document Number<br><b>aPISA2</b> |                                                                                                             | Rev<br><b>1A</b> |
| Date:                                                                                 | Thursday, August 29, 2013        |                                                                                                             | Sheet 42 of 73   |

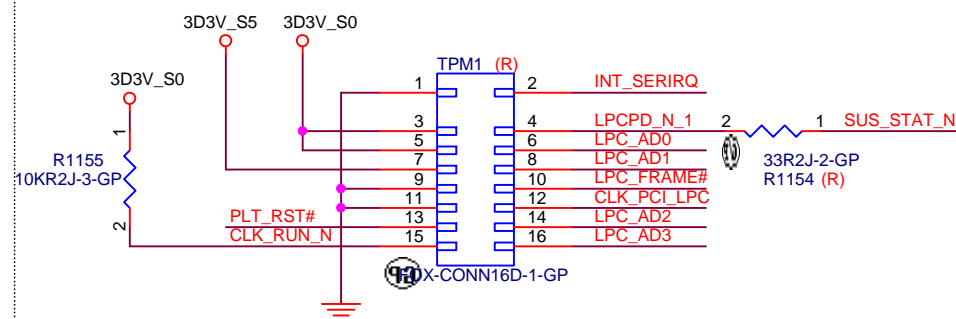




## TPM Header

2012/09/07\_aPisa\_SA  
Add TPM Header

[www.aitech1.ru](http://www.aitech1.ru)



## <Core Design>

緯創資通

# Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

| Title                                                                      | Author        | Year | Journal                       | Volume | Issue | Page    |
|----------------------------------------------------------------------------|---------------|------|-------------------------------|--------|-------|---------|
| 1. The Effect of Temperature on the Rate of Reaction                       | John Doe      | 2018 | Journal of Chemical Education | 95     | 3     | 456-462 |
| 2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide | Jane Smith    | 2017 | Journal of Chemical Education | 94     | 2     | 321-328 |
| 3. The Effect of Concentration on the Rate of Reaction                     | Michael Brown | 2016 | Journal of Chemical Education | 93     | 1     | 123-130 |
| 4. The Effect of Surface Area on the Rate of Reaction                      | Sarah White   | 2015 | Journal of Chemical Education | 92     | 4     | 567-574 |
| 5. The Effect of Catalyst on the Rate of Reaction                          | David Green   | 2014 | Journal of Chemical Education | 91     | 5     | 678-685 |

## **Debug connector**

Size  
A4

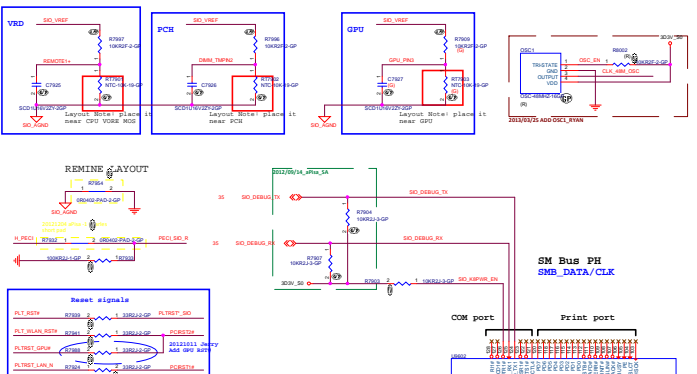
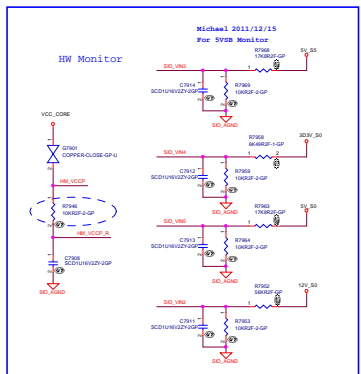
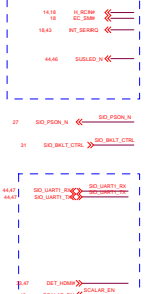
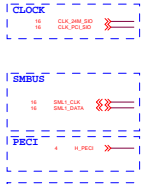
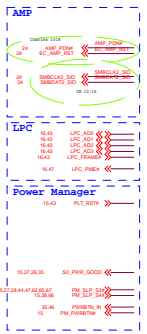
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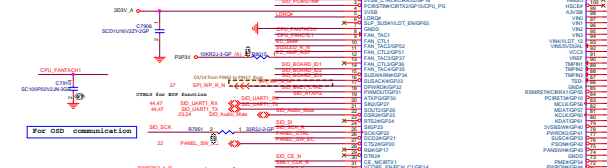
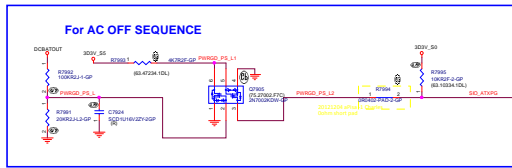
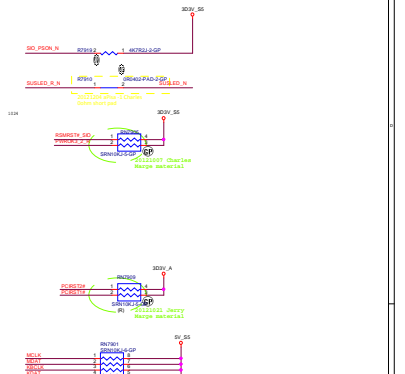




**IT8732 Power On Strapping Options**

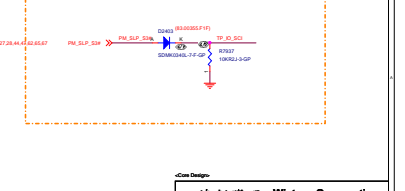
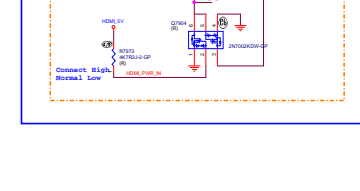
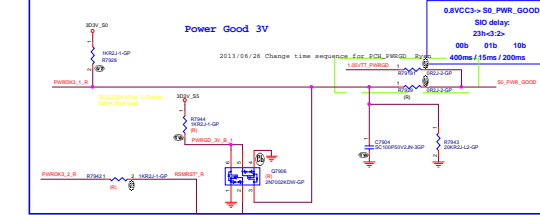
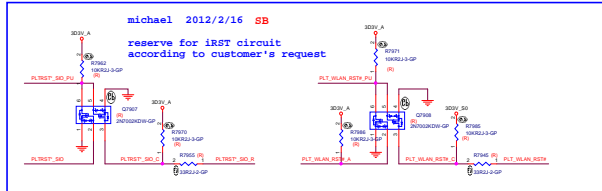
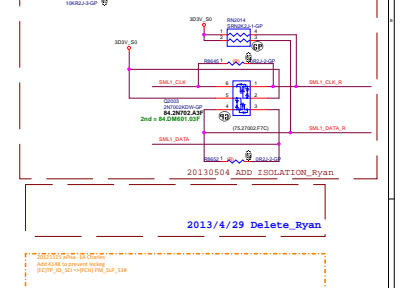
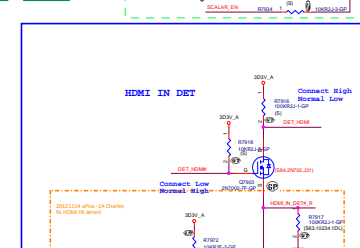
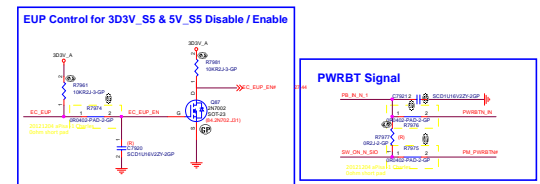
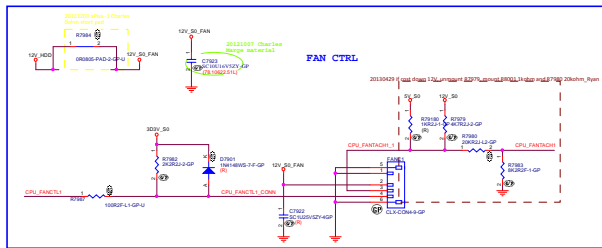
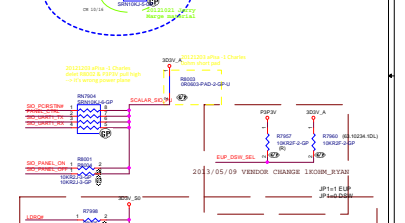
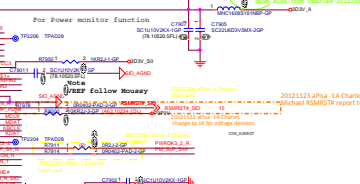
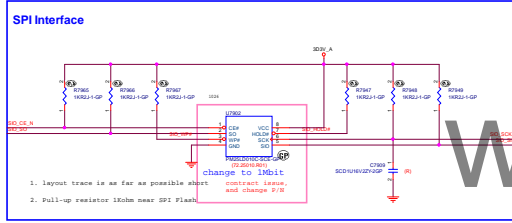
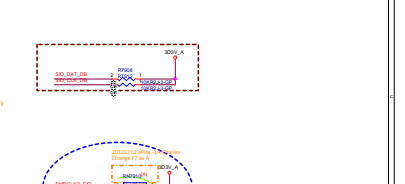
| Symbol | Value        | Description |
|--------|--------------|-------------|
| JP1    | 0SW, EUP_SEL | 1: EUP      |
| Pin 0  | 0: 0SW       | 0: 0SW      |

If without use these pins, Please pull-up to 3.3V.  
Don't let it floating  
Pin19/24/25/30/48/57/71/75/77/80-83/96/95



**SB EC Board ID Description**

| SA | SB | SC | SD | SE |
|----|----|----|----|----|
| 0  | 0  | 0  | 0  | 0  |
| 1  | 1  | 1  | 1  | 1  |
| 2  | 2  | 2  | 2  | 2  |





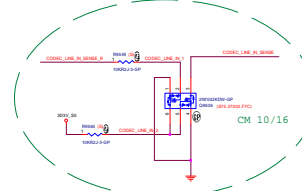
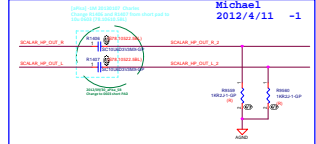
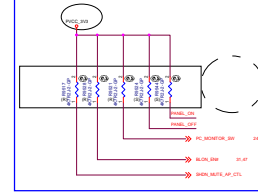
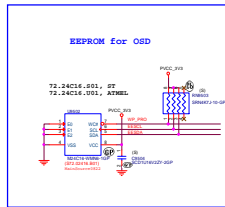
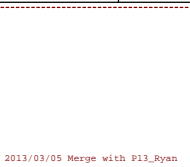
2012/08/18\_aPisa\_SA  
Delete Battery Charger

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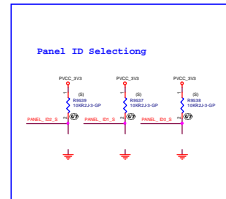
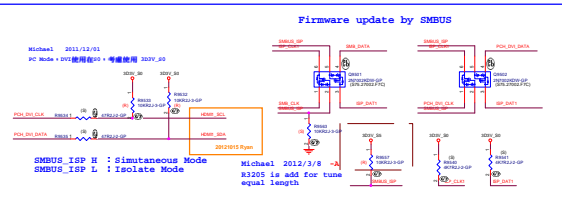
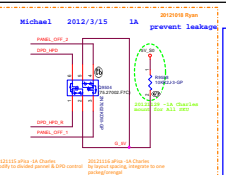


| Monitor mode |            |           |                  |
|--------------|------------|-----------|------------------|
| Monitor      | DET_HDMI18 | SCALAR_EN | Panel EN/PM/CTRL |
|              | 0          | 1         | Active           |

DET\_HDMI18 : connect to SIO and Scalar

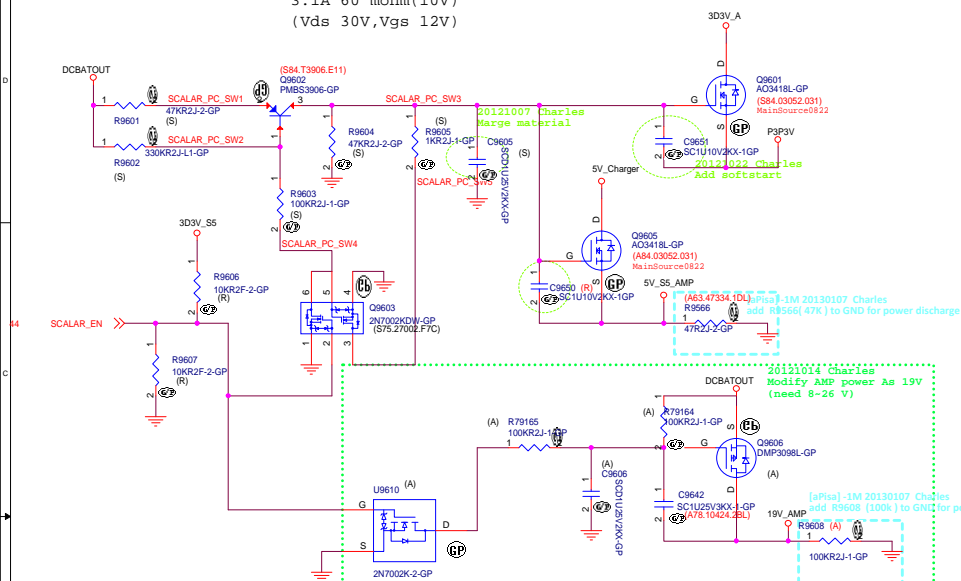
To SIO: make scalar working at SCALAR\_EN 1(From SIO)


To Scalar: Let scalar know HDMI IN, and make related signal active, Panel and MDP





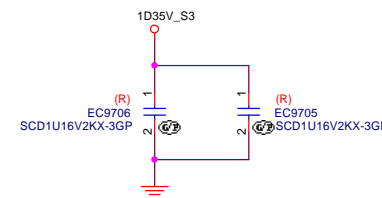
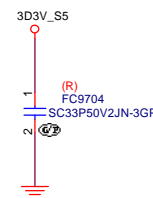
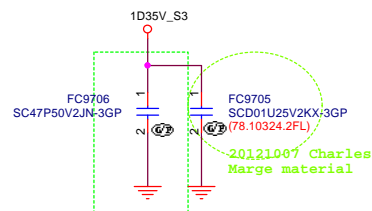
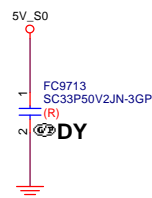
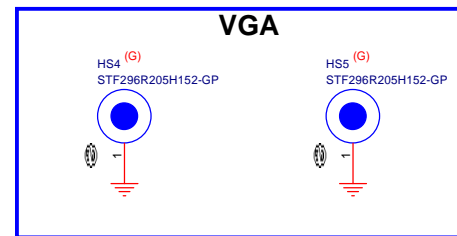
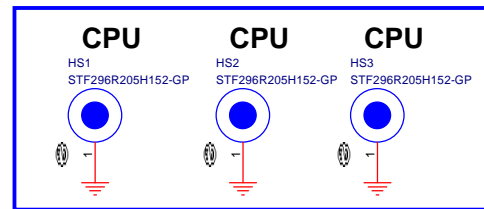
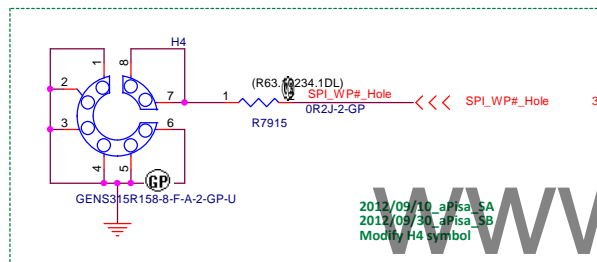
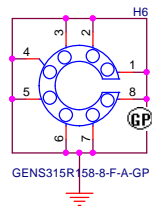
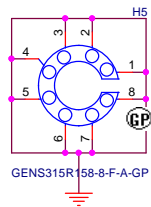
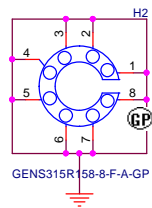
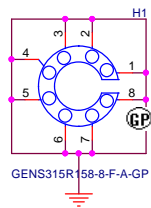
AO3418 NMOS 3.1A, 60mohm,Vgs=10V **Michael 2011/12/01**  
NMOS H: Enable L:Disable **change 5V\_S5 to 5V\_Charger**  
3.1A 60 mohm(10V)  
(Vds 30V,Vgs 12V) 3D3V\_A  
Q



| GPI input |                                                                                                                                          | From | High   | Low     | Default                                       |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------|------|--------|---------|-----------------------------------------------|
| Pin69     | GPI-1 PC Power ON  PM_SLP_S3# 15,27,28,44,47,62,65,67 | SB   | PC     | Monitor | Monitor                                       |
| Pin109    | GPI-2 Mode change/<br>Panel OnOff                                                                                                        | SW   | Normal | Touch   | PC: PC(PC->HDMI)<br>Monitor: HDMI, VGA (HDMI) |

|        |                    |                  |       |        |         |         |                                  |
|--------|--------------------|------------------|-------|--------|---------|---------|----------------------------------|
| Pin55  | GPO-2 Panel On/OFF | SCALAR_VDD_EN    | 31,47 | Scalar | ON      | OFF     | PC: ON<br>Monitor: Detect Signal |
| Pin104 | GPO-3 PC/Monitor   | PC_MONITOR_SW    | 24,48 | Scalar | PC      | Monitor | PC: PC,<br>Monitor: HDMI, VGA    |
| Pin101 | GPO-5 Video        | BLON_EN#         | 31,47 | Scalar | Disable | Enable  | Disable                          |
| Pin72  | GPO-6 Audio Mute   | SHDN_MUTE_AP_CTL | 48    | Scalar | on-Mute | MUTE    | MUTE                             |



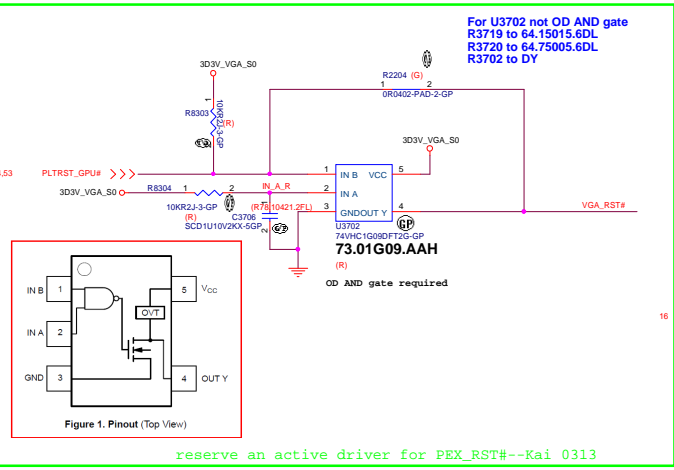


<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title  
**STAND OFF/HOLE/EMI CAP**  
Size A3 Document Number  
**aPISA2** Rev  
**1A**  
Date: Thursday, August 29, 2013 Sheet 49 of 73





reserve an active driver for PEX\_RST#--Kai 0313

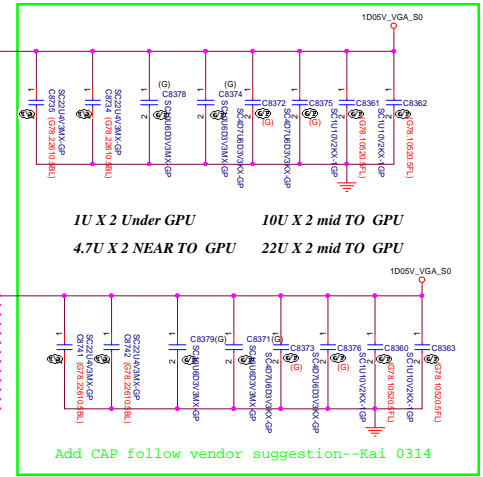
- 14 PEG\_RXP[0..3] <<
- 14 PEG\_RXN[0..3] <<
- 14 PEG\_TXP[0..3] >>
- 14 PEG\_TXN[0..3] >>

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since GPU PCI-E is 8 lanes.--Kai 0313

71.0N14P.A0U  
IC VGA N14P-GV2-B-A1 BGA(GK208-732-A1) --Kai 0313

1U X 2 Under GPU 10U X 2 mid TO GPU  
4.7U X 2 NEAR TO GPU 22U X 2 mid TO GPU



|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

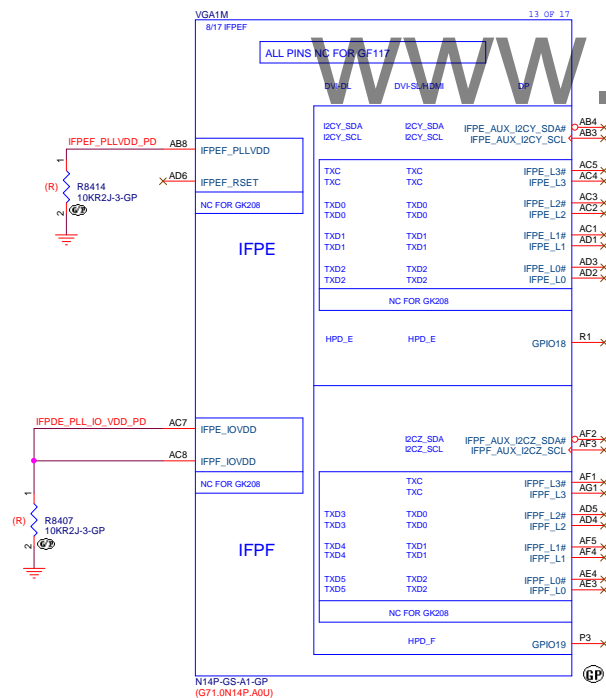
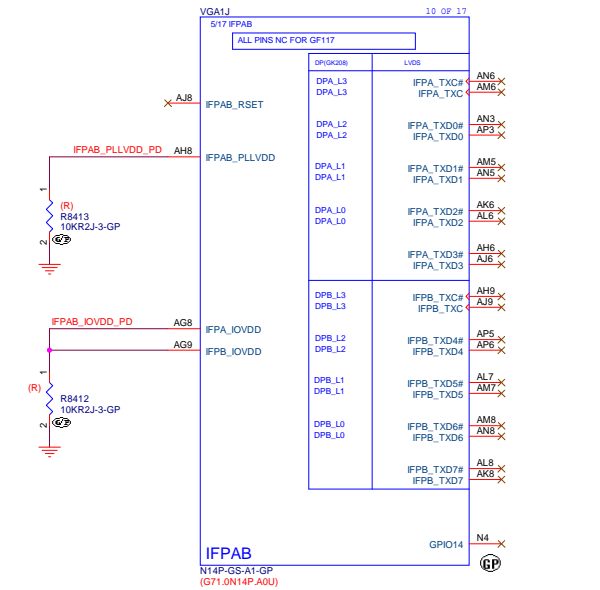
|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |

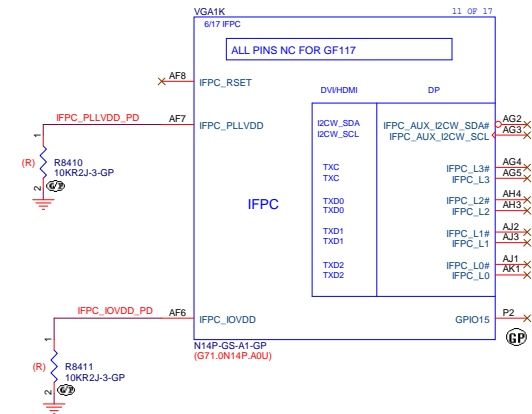
|       |                 |
|-------|-----------------|
| GP108 | GR0308K107GP117 |
| NC    | NC              |



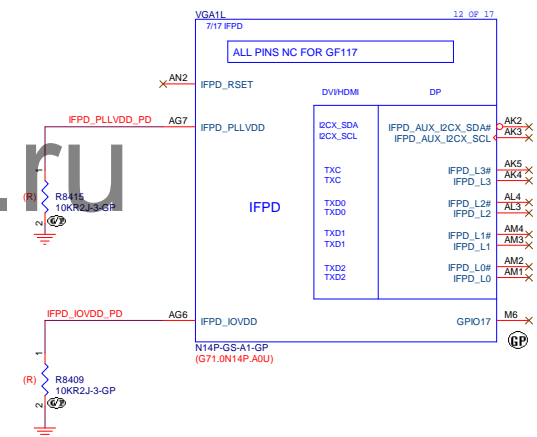
## LVDS Interface



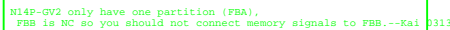
## HDMI Interface



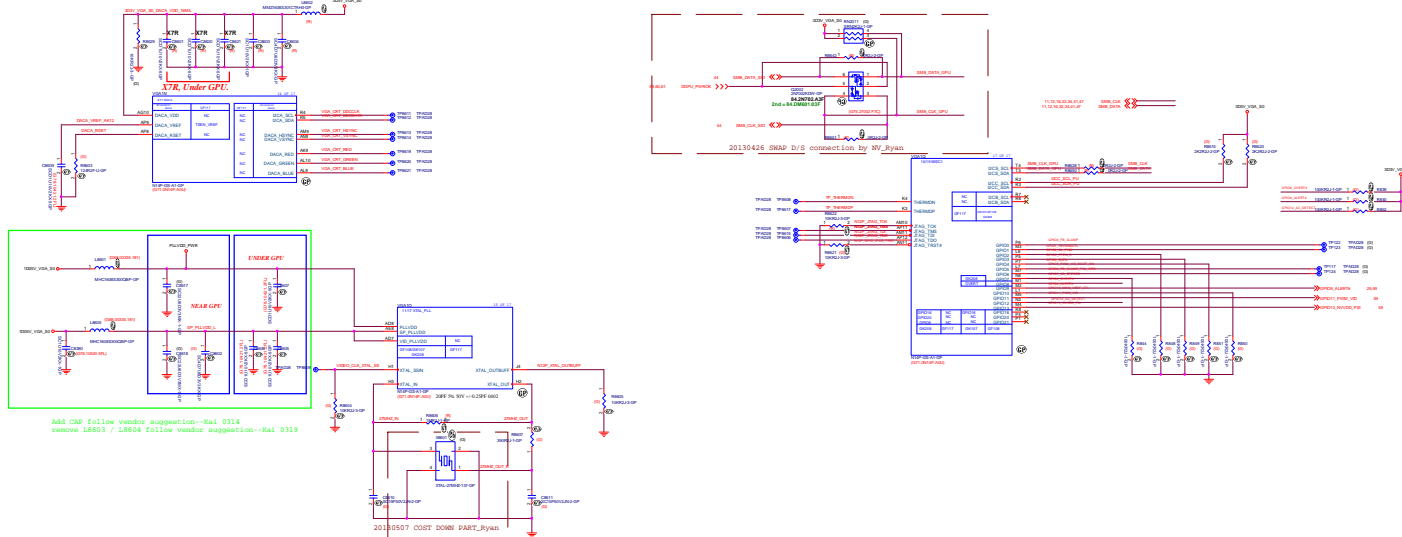
## EDP Interface











Add CAP follow vendor suggestion--Kai 0314  
remove L8603 / L8604 follow vendor suggestion--Kai 0319

20130507 COOT DONG XIAO, Ryan

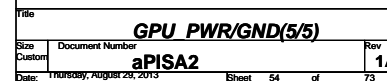
Table 115. GB2+ and GB2-L28 GPU Description

| Pin Name | Normal Function | IO  | Functional Description | Recommended Default Pull-up or Pull-down |
|----------|-----------------|-----|------------------------|------------------------------------------|
| GP00     | PLL_CLAMP_AD0   | 1   | PLL Clamp monitor      | None                                     |
| GP01     | MEM_VDD_CTL     | 2   | Memory VDD_CTL         | None                                     |
| GP02     | LOCAL_PAN       | 3   | Local Panel            | None                                     |
| GP03     | LOCAL_PAN       | 4   | Local Panel            | None                                     |
| GP04     | LOCAL_PAN       | 5   | Local Panel            | None                                     |
| GP05     | LOCAL_PAN       | 6   | Local Panel            | None                                     |
| GP06     | LOCAL_PAN       | 7   | Local Panel            | None                                     |
| GP07     | LOCAL_PAN       | 8   | Local Panel            | None                                     |
| GP08     | LOCAL_PAN       | 9   | Local Panel            | None                                     |
| GP09     | LOCAL_PAN       | 10  | Local Panel            | None                                     |
| GP10     | LOCAL_PAN       | 11  | Local Panel            | None                                     |
| GP11     | LOCAL_PAN       | 12  | Local Panel            | None                                     |
| GP12     | LOCAL_PAN       | 13  | Local Panel            | None                                     |
| GP13     | LOCAL_PAN       | 14  | Local Panel            | None                                     |
| GP14     | LOCAL_PAN       | 15  | Local Panel            | None                                     |
| GP15     | LOCAL_PAN       | 16  | Local Panel            | None                                     |
| GP16     | LOCAL_PAN       | 17  | Local Panel            | None                                     |
| GP17     | LOCAL_PAN       | 18  | Local Panel            | None                                     |
| GP18     | LOCAL_PAN       | 19  | Local Panel            | None                                     |
| GP19     | LOCAL_PAN       | 20  | Local Panel            | None                                     |
| GP20     | LOCAL_PAN       | 21  | Local Panel            | None                                     |
| GP21     | LOCAL_PAN       | 22  | Local Panel            | None                                     |
| GP22     | LOCAL_PAN       | 23  | Local Panel            | None                                     |
| GP23     | LOCAL_PAN       | 24  | Local Panel            | None                                     |
| GP24     | LOCAL_PAN       | 25  | Local Panel            | None                                     |
| GP25     | LOCAL_PAN       | 26  | Local Panel            | None                                     |
| GP26     | LOCAL_PAN       | 27  | Local Panel            | None                                     |
| GP27     | LOCAL_PAN       | 28  | Local Panel            | None                                     |
| GP28     | LOCAL_PAN       | 29  | Local Panel            | None                                     |
| GP29     | LOCAL_PAN       | 30  | Local Panel            | None                                     |
| GP30     | LOCAL_PAN       | 31  | Local Panel            | None                                     |
| GP31     | LOCAL_PAN       | 32  | Local Panel            | None                                     |
| GP32     | LOCAL_PAN       | 33  | Local Panel            | None                                     |
| GP33     | LOCAL_PAN       | 34  | Local Panel            | None                                     |
| GP34     | LOCAL_PAN       | 35  | Local Panel            | None                                     |
| GP35     | LOCAL_PAN       | 36  | Local Panel            | None                                     |
| GP36     | LOCAL_PAN       | 37  | Local Panel            | None                                     |
| GP37     | LOCAL_PAN       | 38  | Local Panel            | None                                     |
| GP38     | LOCAL_PAN       | 39  | Local Panel            | None                                     |
| GP39     | LOCAL_PAN       | 40  | Local Panel            | None                                     |
| GP40     | LOCAL_PAN       | 41  | Local Panel            | None                                     |
| GP41     | LOCAL_PAN       | 42  | Local Panel            | None                                     |
| GP42     | LOCAL_PAN       | 43  | Local Panel            | None                                     |
| GP43     | LOCAL_PAN       | 44  | Local Panel            | None                                     |
| GP44     | LOCAL_PAN       | 45  | Local Panel            | None                                     |
| GP45     | LOCAL_PAN       | 46  | Local Panel            | None                                     |
| GP46     | LOCAL_PAN       | 47  | Local Panel            | None                                     |
| GP47     | LOCAL_PAN       | 48  | Local Panel            | None                                     |
| GP48     | LOCAL_PAN       | 49  | Local Panel            | None                                     |
| GP49     | LOCAL_PAN       | 50  | Local Panel            | None                                     |
| GP50     | LOCAL_PAN       | 51  | Local Panel            | None                                     |
| GP51     | LOCAL_PAN       | 52  | Local Panel            | None                                     |
| GP52     | LOCAL_PAN       | 53  | Local Panel            | None                                     |
| GP53     | LOCAL_PAN       | 54  | Local Panel            | None                                     |
| GP54     | LOCAL_PAN       | 55  | Local Panel            | None                                     |
| GP55     | LOCAL_PAN       | 56  | Local Panel            | None                                     |
| GP56     | LOCAL_PAN       | 57  | Local Panel            | None                                     |
| GP57     | LOCAL_PAN       | 58  | Local Panel            | None                                     |
| GP58     | LOCAL_PAN       | 59  | Local Panel            | None                                     |
| GP59     | LOCAL_PAN       | 60  | Local Panel            | None                                     |
| GP60     | LOCAL_PAN       | 61  | Local Panel            | None                                     |
| GP61     | LOCAL_PAN       | 62  | Local Panel            | None                                     |
| GP62     | LOCAL_PAN       | 63  | Local Panel            | None                                     |
| GP63     | LOCAL_PAN       | 64  | Local Panel            | None                                     |
| GP64     | LOCAL_PAN       | 65  | Local Panel            | None                                     |
| GP65     | LOCAL_PAN       | 66  | Local Panel            | None                                     |
| GP66     | LOCAL_PAN       | 67  | Local Panel            | None                                     |
| GP67     | LOCAL_PAN       | 68  | Local Panel            | None                                     |
| GP68     | LOCAL_PAN       | 69  | Local Panel            | None                                     |
| GP69     | LOCAL_PAN       | 70  | Local Panel            | None                                     |
| GP70     | LOCAL_PAN       | 71  | Local Panel            | None                                     |
| GP71     | LOCAL_PAN       | 72  | Local Panel            | None                                     |
| GP72     | LOCAL_PAN       | 73  | Local Panel            | None                                     |
| GP73     | LOCAL_PAN       | 74  | Local Panel            | None                                     |
| GP74     | LOCAL_PAN       | 75  | Local Panel            | None                                     |
| GP75     | LOCAL_PAN       | 76  | Local Panel            | None                                     |
| GP76     | LOCAL_PAN       | 77  | Local Panel            | None                                     |
| GP77     | LOCAL_PAN       | 78  | Local Panel            | None                                     |
| GP78     | LOCAL_PAN       | 79  | Local Panel            | None                                     |
| GP79     | LOCAL_PAN       | 80  | Local Panel            | None                                     |
| GP80     | LOCAL_PAN       | 81  | Local Panel            | None                                     |
| GP81     | LOCAL_PAN       | 82  | Local Panel            | None                                     |
| GP82     | LOCAL_PAN       | 83  | Local Panel            | None                                     |
| GP83     | LOCAL_PAN       | 84  | Local Panel            | None                                     |
| GP84     | LOCAL_PAN       | 85  | Local Panel            | None                                     |
| GP85     | LOCAL_PAN       | 86  | Local Panel            | None                                     |
| GP86     | LOCAL_PAN       | 87  | Local Panel            | None                                     |
| GP87     | LOCAL_PAN       | 88  | Local Panel            | None                                     |
| GP88     | LOCAL_PAN       | 89  | Local Panel            | None                                     |
| GP89     | LOCAL_PAN       | 90  | Local Panel            | None                                     |
| GP90     | LOCAL_PAN       | 91  | Local Panel            | None                                     |
| GP91     | LOCAL_PAN       | 92  | Local Panel            | None                                     |
| GP92     | LOCAL_PAN       | 93  | Local Panel            | None                                     |
| GP93     | LOCAL_PAN       | 94  | Local Panel            | None                                     |
| GP94     | LOCAL_PAN       | 95  | Local Panel            | None                                     |
| GP95     | LOCAL_PAN       | 96  | Local Panel            | None                                     |
| GP96     | LOCAL_PAN       | 97  | Local Panel            | None                                     |
| GP97     | LOCAL_PAN       | 98  | Local Panel            | None                                     |
| GP98     | LOCAL_PAN       | 99  | Local Panel            | None                                     |
| GP99     | LOCAL_PAN       | 100 | Local Panel            | None                                     |

GP000 and GP001 are only available on H14M-GP1-GE1-GE2-GE3-GE4-GE5-GE6-GE7-GE8-GE9-GE10-GE11-GE12-GE13-GE14-GE15-GE16-GE17-GE18-GE19-GE20-GE21-GE22-GE23-GE24-GE25-GE26-GE27-GE28-GE29-GE30-GE31-GE32-GE33-GE34-GE35-GE36-GE37-GE38-GE39-GE40-GE41-GE42-GE43-GE44-GE45-GE46-GE47-GE48-GE49-GE50-GE51-GE52-GE53-GE54-GE55-GE56-GE57-GE58-GE59-GE60-GE61-GE62-GE63-GE64-GE65-GE66-GE67-GE68-GE69-GE70-GE71-GE72-GE73-GE74-GE75-GE76-GE77-GE78-GE79-GE80-GE81-GE82-GE83-GE84-GE85-GE86-GE87-GE88-GE89-GE90-GE91-GE92-GE93-GE94-GE95-GE96-GE97-GE98-GE99-GE100-GE101-GE102-GE103-GE104-GE105-GE106-GE107-GE108-GE109-GE110-GE111-GE112-GE113-GE114-GE115-GE116-GE117-GE118-GE119-GE120-GE121-GE122-GE123-GE124-GE125-GE126-GE127-GE128-GE129-GE130-GE131-GE132-GE133-GE134-GE135-GE136-GE137-GE138-GE139-GE140-GE141-GE142-GE143-GE144-GE145-GE146-GE147-GE148-GE149-GE150-GE151-GE152-GE153-GE154-GE155-GE156-GE157-GE158-GE159-GE160-GE161-GE162-GE163-GE164-GE165-GE166-GE167-GE168-GE169-GE170-GE171-GE172-GE173-GE174-GE175-GE176-GE177-GE178-GE179-GE180-GE181-GE182-GE183-GE184-GE185-GE186-GE187-GE188-GE189-GE190-GE191-GE192-GE193-GE194-GE195-GE196-GE197-GE198-GE199-GE200-GE201-GE202-GE203-GE204-GE205-GE206-GE207-GE208-GE209-GE210-GE211-GE212-GE213-GE214-GE215-GE216-GE217-GE218-GE219-GE220-GE221-GE222-GE223-GE224-GE225-GE226-GE227-GE228-GE229-GE230-GE231-GE232-GE233-GE234-GE235-GE236-GE237-GE238-GE239-GE240-GE241-GE242-GE243-GE244-GE245-GE246-GE247-GE248-GE249-GE250-GE251-GE252-GE253-GE254-GE255-GE256-GE257-GE258-GE259-GE260-GE261-GE262-GE263-GE264-GE265-GE266-GE267-GE268-GE269-GE270-GE271-GE272-GE273-GE274-GE275-GE276-GE277-GE278-GE279-GE280-GE281-GE282-GE283-GE284-GE285-GE286-GE287-GE288-GE289-GE290-GE291-GE292-GE293-GE294-GE295-GE296-GE297-GE298-GE299-GE300-GE301-GE302-GE303-GE304-GE305-GE306-GE307-GE308-GE309-GE310-GE311-GE312-GE313-GE314-GE315-GE316-GE317-GE318-GE319-GE320-GE321-GE322-GE323-GE324-GE325-GE326-GE327-GE328-GE329-GE330-GE331-GE332-GE333-GE334-GE335-GE336-GE337-GE338-GE339-GE340-GE341-GE342-GE343-GE344-GE345-GE346-GE347-GE348-GE349-GE350-GE351-GE352-GE353-GE354-GE355-GE356-GE357-GE358-GE359-GE360-GE361-GE362-GE363-GE364-GE365-GE366-GE367-GE368-GE369-GE370-GE371-GE372-GE373-GE374-GE375-GE376-GE377-GE378-GE379-GE380-GE381-GE382-GE383-GE384-GE385-GE386-GE387-GE388-GE389-GE390-GE391-GE392-GE393-GE394-GE395-GE396-GE397-GE398-GE399-GE400-GE401-GE402-GE403-GE404-GE405-GE406-GE407-GE408-GE409-GE410-GE411-GE412-GE413-GE414-GE415-GE416-GE417-GE418-GE419-GE420-GE421-GE422-GE423-GE424-GE425-GE426-GE427-GE428-GE429-GE430-GE431-GE432-GE433-GE434-GE435-GE436-GE437-GE438-GE439-GE440-GE441-GE442-GE443-GE444-GE445-GE446-GE447-GE448-GE449-GE450-GE451-GE452-GE453-GE454-GE455-GE456-GE457-GE458-GE459-GE460-GE461-GE462-GE463-GE464-GE465-GE466-GE467-GE468-GE469-GE470-GE471-GE472-GE473-GE474-GE475-GE476-GE477-GE478-GE479-GE480-GE481-GE482-GE483-GE484-GE485-GE486-GE487-GE488-GE489-GE490-GE491-GE492-GE493-GE494-GE495-GE496-GE497-GE498-GE499-GE500-GE501-GE502-GE503-GE504-GE505-GE506-GE507-GE508-GE509-GE510-GE511-GE512-GE513-GE514-GE515-GE516-GE517-GE518-GE519-GE520-GE521-GE522-GE523-GE524-GE525-GE526-GE527-GE528-GE529-GE530-GE531-GE532-GE533-GE534-GE535-GE536-GE537-GE538-GE539-GE540-GE541-GE542-GE543-GE544-GE545-GE546-GE547-GE548-GE549-GE550-GE551-GE552-GE553-GE554-GE555-GE556-GE557-GE558-GE559-GE560-GE561-GE562-GE563-GE564-GE565-GE566-GE567-GE568-GE569-GE570-GE571-GE572-GE573-GE574-GE575-GE576-GE577-GE578-GE579-GE580-GE581-GE582-GE583-GE584-GE585-GE586-GE587-GE588-GE589-GE590-GE591-GE592-GE593-GE594-GE595-GE596-GE597-GE598-GE599-GE600-GE601-GE602-GE603-GE604-GE605-GE606-GE607-GE608-GE609-GE610-GE611-GE612-GE613-GE614-GE615-GE616-GE617-GE618-GE619-GE620-GE621-GE622-GE623-GE624-GE625-GE626-GE627-GE628-GE629-GE630-GE631-GE632-GE633-GE634-GE635-GE636-GE637-GE638-GE639-GE640-GE641-GE642-GE643-GE644-GE645-GE646-GE647-GE648-GE649-GE650-GE651-GE652-GE653-GE654-GE655-GE656-GE657-GE658-GE659-GE660-GE661-GE662-GE663-GE664-GE665-GE666-GE667-GE668-GE669-GE670-GE671-GE672-GE673-GE674-GE675-GE676-GE677-GE678-GE679-GE680-GE681-GE682-GE683-GE684-GE685-GE686-GE687-GE688-GE689-GE690-GE691-GE692-GE693-GE694-GE695-GE696-GE697-GE698-GE699-GE700-GE701-GE702-GE703-GE704-GE705-GE706-GE707-GE708-GE709-GE710-GE711-GE712-GE713-GE714-GE715-GE716-GE717-GE718-GE719-GE720-GE721-GE722-GE723-GE724-GE725-GE726-GE727-GE728-GE729-GE730-GE731-GE732-GE733-GE734-GE735-GE736-GE737-GE738-GE739-GE740-GE741-GE742-GE743-GE744-GE745-GE746-GE747-GE748-GE749-GE750-GE751-GE752-GE753-GE754-GE755-GE756-GE757-GE758-GE759-GE760-GE761-GE762-GE763-GE764-GE765-GE766-GE767-GE768-GE769-GE770-GE771-GE772-GE773-GE774-GE775-GE776-GE777-GE778-GE779-GE780-GE781-GE782-GE783-GE784-GE785-GE786-GE787-GE788-GE789-GE790-GE791-GE792-GE793-GE794-GE795-GE796-GE797-GE798-GE799-GE800-GE801-GE802-GE803-GE804-GE805-GE806-GE807-GE808-GE809-GE810-GE811-GE812-GE813-GE814-GE815-GE816-GE817-GE818-GE819-GE820-GE821-GE822-GE823-GE824-GE825-GE826-GE827-GE828-GE829-GE830-GE831-GE832-GE833-GE834-GE835-GE836-GE837-GE838-GE839-GE840-GE841-GE842-GE843-GE844-GE845-GE846-GE847-GE848-GE849-GE850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## VGA\_CORE

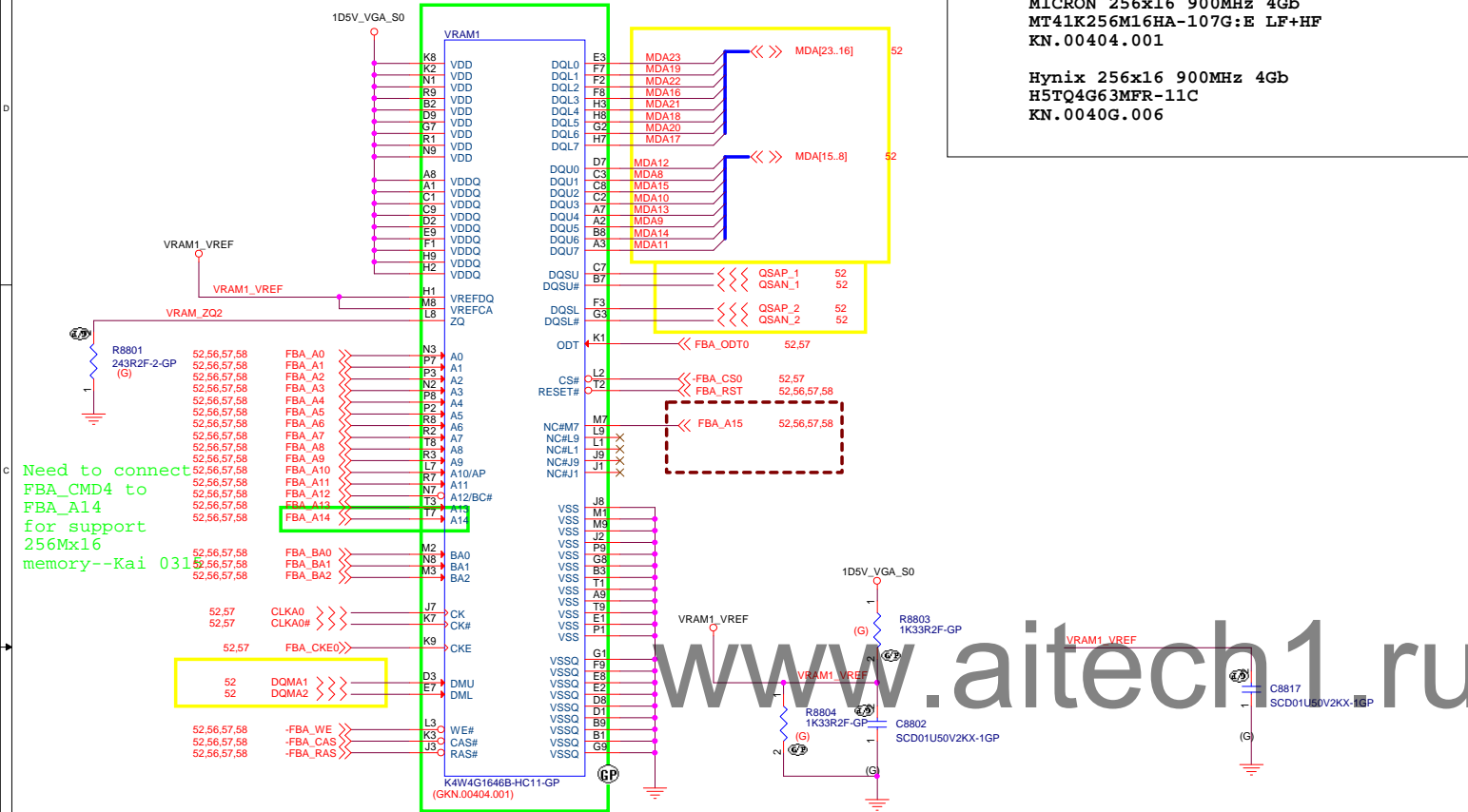




## CHANNEL A:2GB DDR3

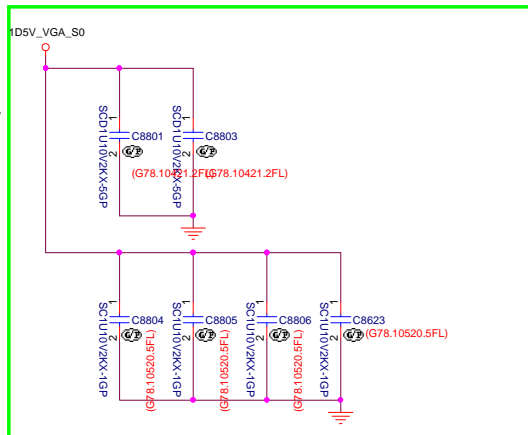
MICRON 256x16 900MHz 4Gb  
MT41K256M16HA-107G:E LF+HF  
KN.00404.001

Hynix 256x16 900MHz 4Gb  
H5TQ4G63MFR-11C  
KN.0040G.006



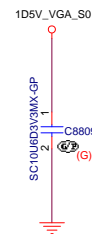
OBS, follow Lily\_Tripoli--Kai 0311

FOR VRAM1



Add VRAM decoupling cap--Kai 0315

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



CLOSE TO THE MEMORY

<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

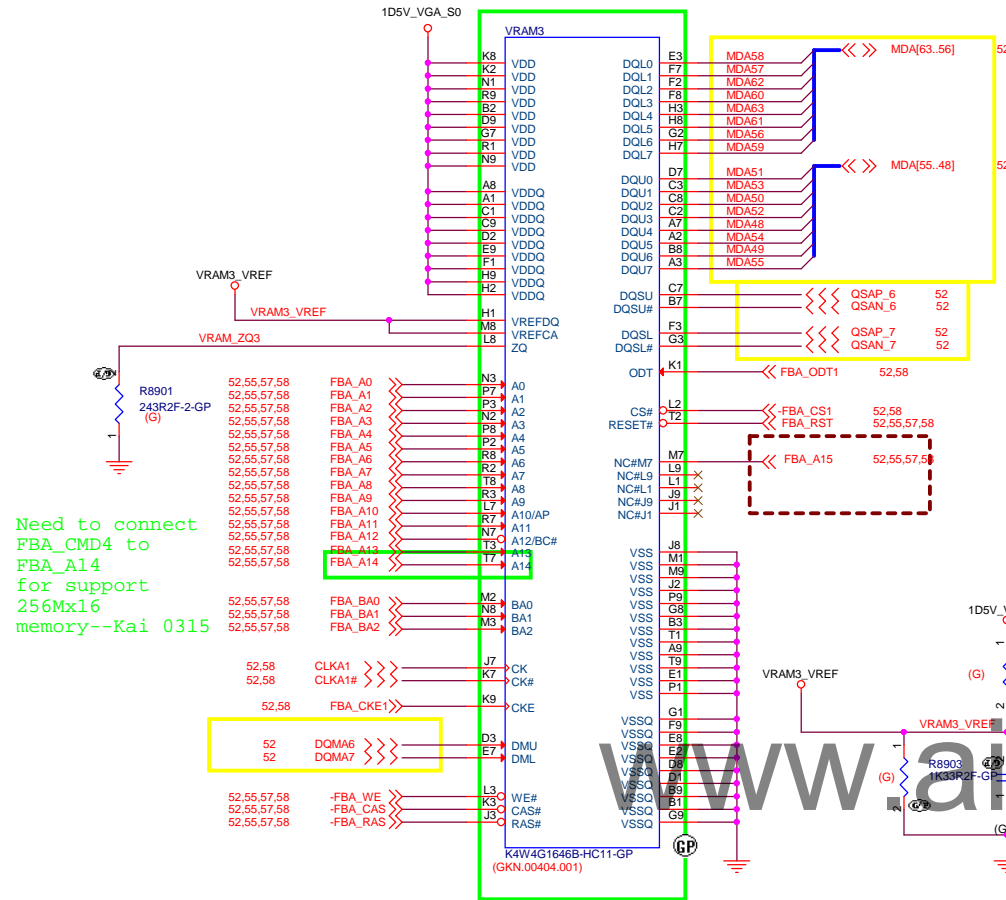
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|-----------------|---------------------------|-------|----------|
| Size            | Document Number           |       | Rev      |
| Custom          | aPISA2                    |       | 1A       |
| Date:           | Thursday, August 29, 2013 | Sheet | 55 of 73 |



# CHANNEL A:2GB DDR3

MICRON 256x16 900MHz 4Gb  
MT41K256M16HA-107G:E LF+HF  
KN.00404.001

Hynix 256x16 900MHz 4Gb  
H5TQ4G63MFR-11C  
KN.0040G.006



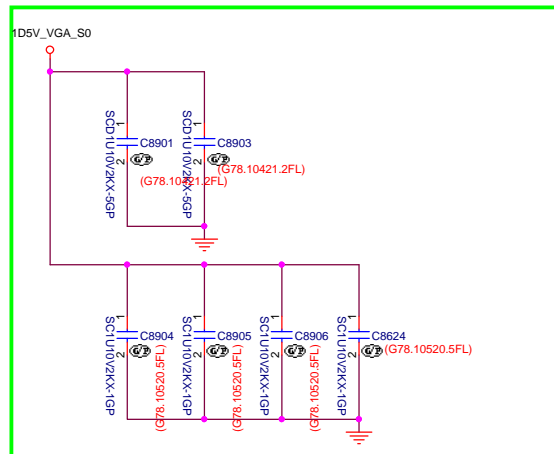
OBS,follow Lily\_Tripoli--Kai 0311

FB CMD mapping Mode D-N12x

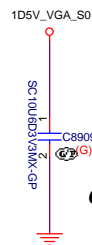
VRAM SAMSUNG 1Gb S72.41646.Q0U  
VRAM HYNIX 1Gb H72.51G63.H0U

FOR VRAM3

CLOSE TO THE MEMORY



Add VRAM decoupling cap--Kai 0315



CLOSE TO THE MEMORY

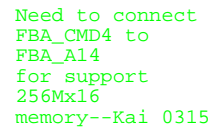
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緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipet Hsien 221, Taiwan, R.O.C.

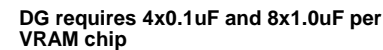
|        |                           |       |                 |
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| Title  |                           |       | GPU-VRAM3 (2/4) |
| Size   | Document Number           | Rev   |                 |
| Custom | aPISA2                    | 1A    |                 |
| Date:  | Thursday, August 29, 2013 | Sheet | 56 of 73        |



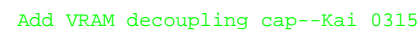
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H5TQ4G63MFR-11C
KN.0040G.006
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## CLOSE TO THE MEMORY





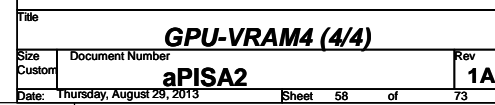




Table 1. PWM-VID Spec and Component Values

| PWM-VID Spec                       |          |          |          |       |
|------------------------------------|----------|----------|----------|-------|
|                                    | Config A | Config B | Config C |       |
| Vmin                               | V        | 0.6      | 0.6      | 0.65  |
| Vmax                               | V        | 1.2      | 1.2      | 1.15  |
| Vboot                              | V        | 0.875    | 0.9      | 0.9   |
| Voltage Step Vstep                 | mV       | 6.25     | 6.25     | 25    |
| Number of Voltage Levels N         | level    | 96       | 96       | 20    |
| PWM Frequency $F_{PWM}$            | MHz      | 1.125    | 1.125    | 0.676 |
| PWM Minimum Pulse Width $T_{DMIN}$ | ns       | 9.26     | 9.26     | 74    |
| VID Transient Time T               | us       | <100     | <100     | <100  |
| Component Value                    |          |          |          |       |
| R1 (1%)                            | KQ       | 39       | 20       | 39    |
| R2 (1%)                            | KQ       | 39       | 20       | 30    |
| R3 (1%)                            | KQ       | 1.5      | 2        | 3     |
| R4 (1%)                            | KQ       | 30       | 18       | 24    |
| R5 (1%)                            | KQ       | 1.5      | 0        | 3     |
| C                                  | nF       | 1.5      | 2.7      | 1.8   |

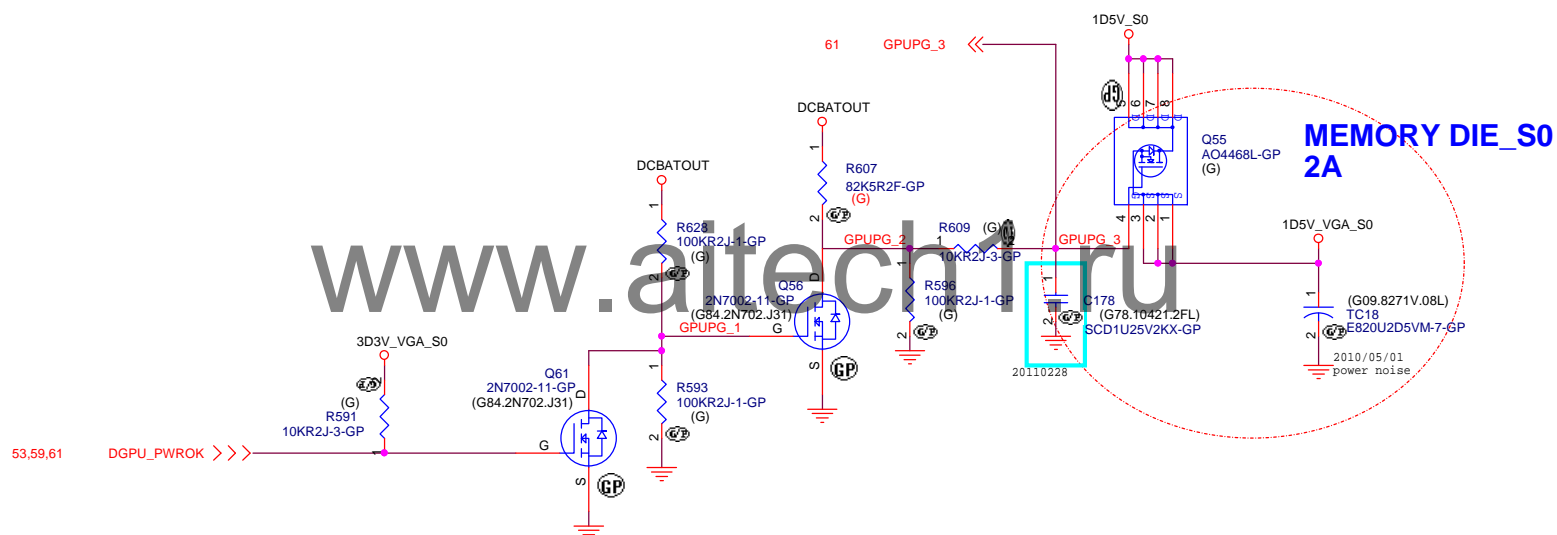
| nvidia          | Pisa2       | nvidia          | Pisa2       |
|-----------------|-------------|-----------------|-------------|
| Config B (N14P) | N14P        | Config C (N14M) | N14M        |
| R1=20K          | PR995=20K   | R1=39K          | PR995=39K   |
| R2=20K          | PR994=20K   | R2=30K          | PR994=30K   |
| R3=2K           | PR9238=2K   | R3=3K           | PR9238=3K   |
| R4=18K          | PR992A=18K  | R4=24K          | PR992A=24K  |
| R5=0            | NA          | R5=3K           | NA          |
| C=2.7nF         | PC615=2.7nF | C=1.8nF         | PC615=1.8nF |

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1D5V\_VGA\_S0  
MAX=6A

GPU VCORE -> MEMORY POWER



<Variant Name>

**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

|                                |                           |                |           |
|--------------------------------|---------------------------|----------------|-----------|
| Title                          |                           |                |           |
| <b>GPU PWR 1D5V VGA(51363)</b> |                           |                |           |
| Size B                         | Document Number           |                | Rev       |
|                                | <b>aPISA2</b>             |                | <b>1A</b> |
| Date:                          | Thursday, August 29, 2013 | Sheet 60 of 73 |           |



# Power Sequencing Requirement N14P-GV2-B-A1

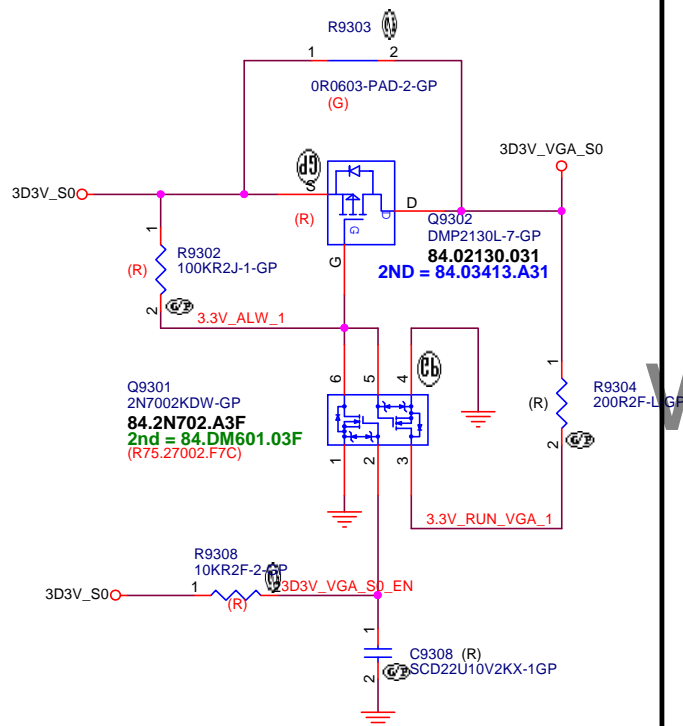
Power-on:

3D3V\_VGA\_S0-->NVVDD-->1D5V\_VGA\_S0-->1D05V\_VGA\_S0

Power-off:

The timing of all power rail need power down to 0V under 10ms.

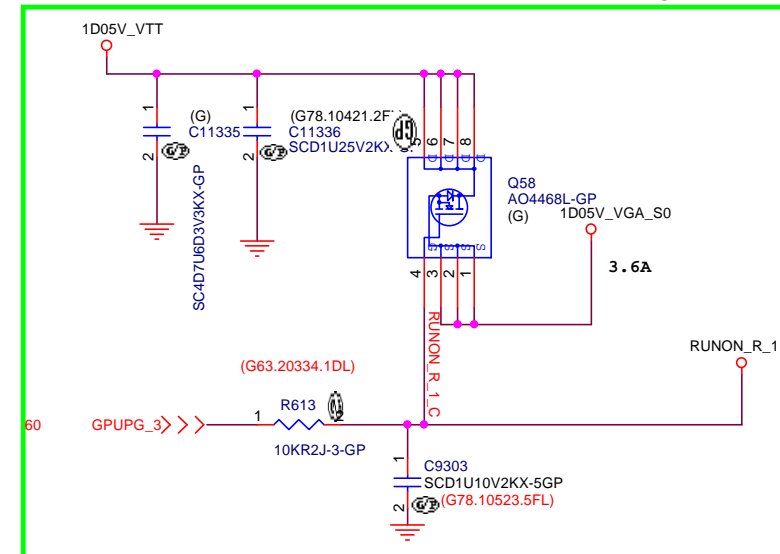
## +3VS to 3.3V\_DELAY Transfer



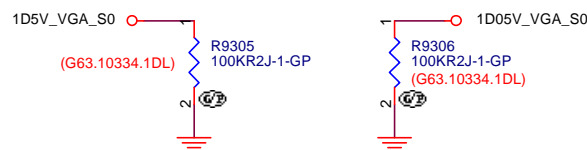
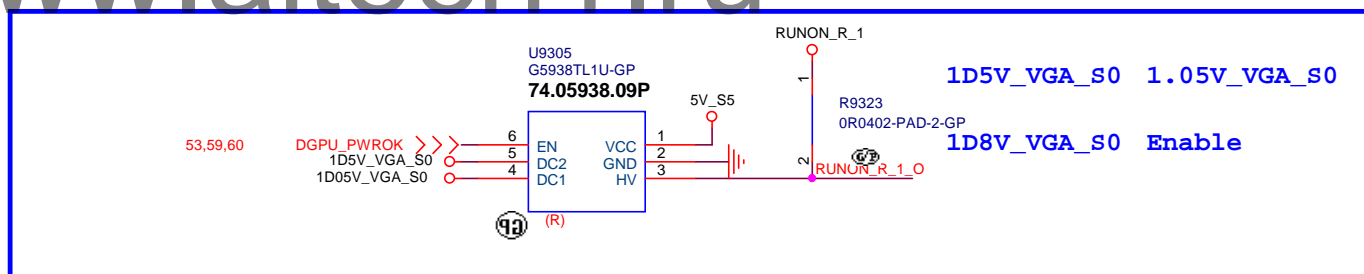
Del 1D5V to 1.D5V\_VGA\_S0 Transfer  
move to page 62--Kai 0313

## 1.05V to 1.05V\_VGA\_S0 Transfer

FDMS0310, POWER PAK  
Max Rdson=3.5m ohm at Vgs=10V,21A



Change U9302 to SOP-8 package, AO6402A Rdson is too large. Please change to use Rdson less than 5m ohm part.--Kai 0315



<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU PWR 1D05V/3D3V

Size

Document Number

aPISA2

Rev

1A

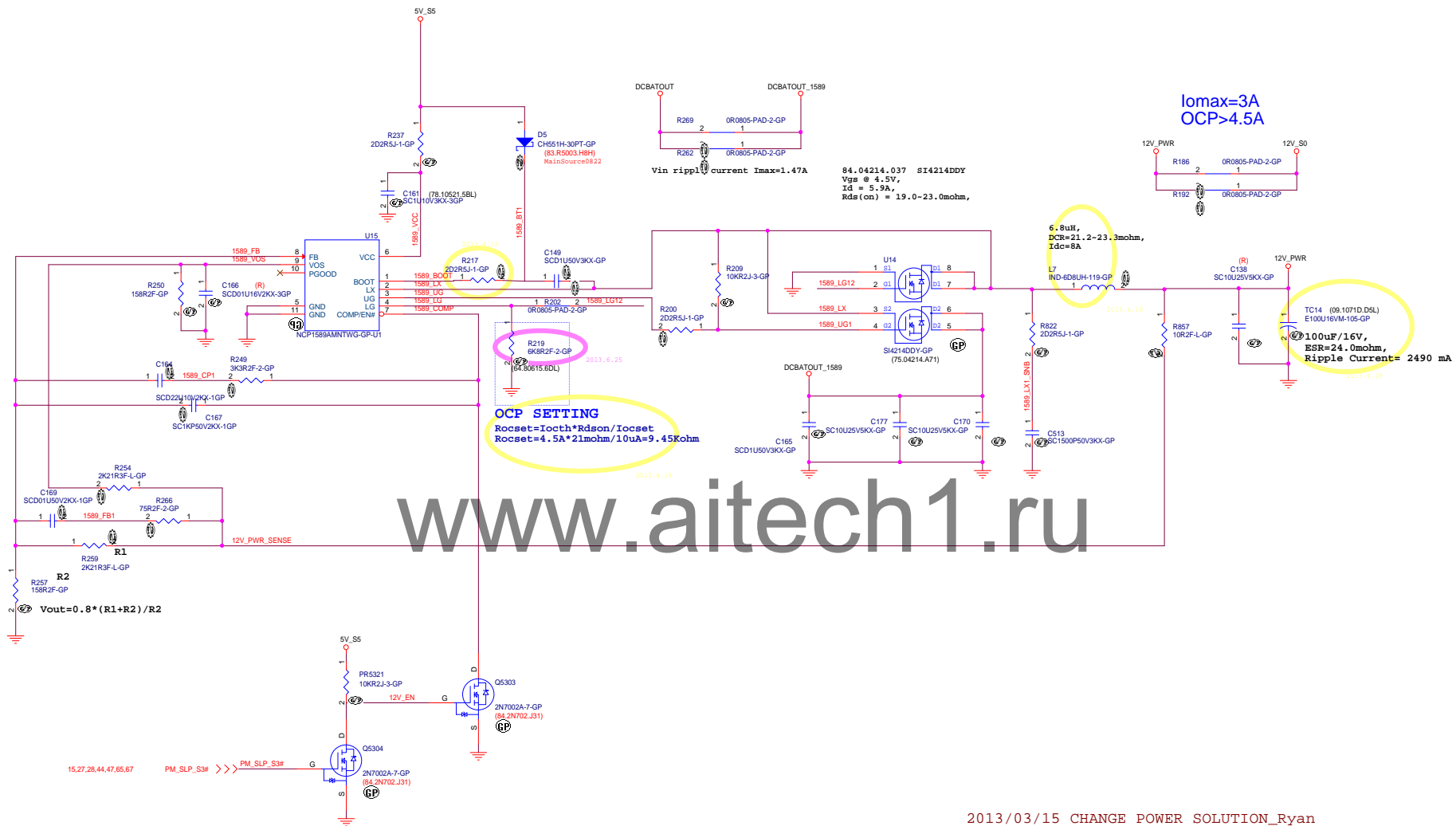
Date: Thursday, August 29, 2013

Sheet 61

of

73





2013/03/15 CHANGE POWER SOLUTION\_Ryan

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

12V

Size

**aPIS**

Date: Thursday, August 29, 2013

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Sheet

62

of \_\_\_\_\_

73

12V

Size

3

Date:

---

Sheet

62

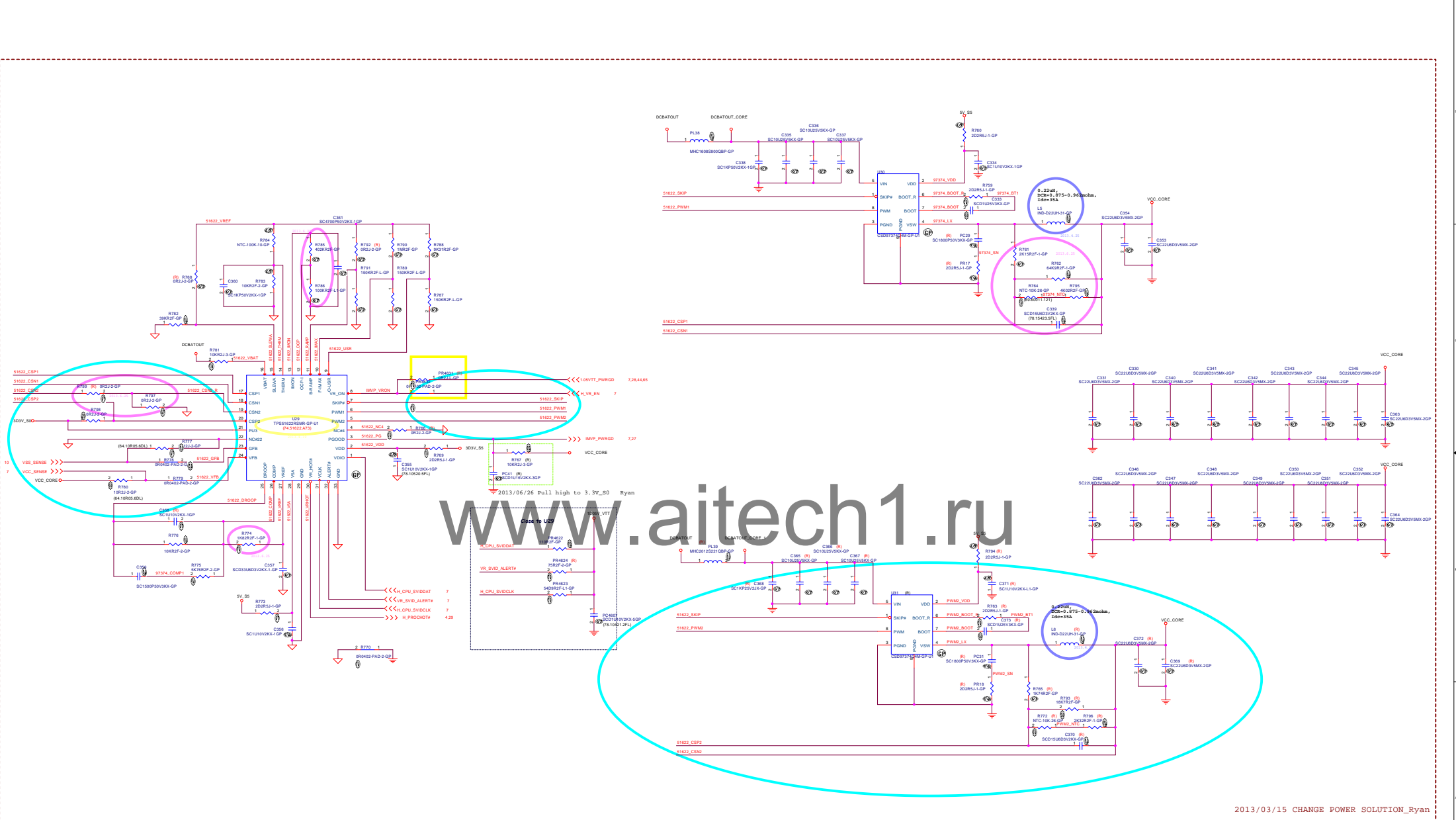
of \_\_\_\_\_

73









2013/03/15 CHANGE POWER SOLUTION\_Ryan



# 1D05V\_VTT

2013.4.2 Modify\_Shang

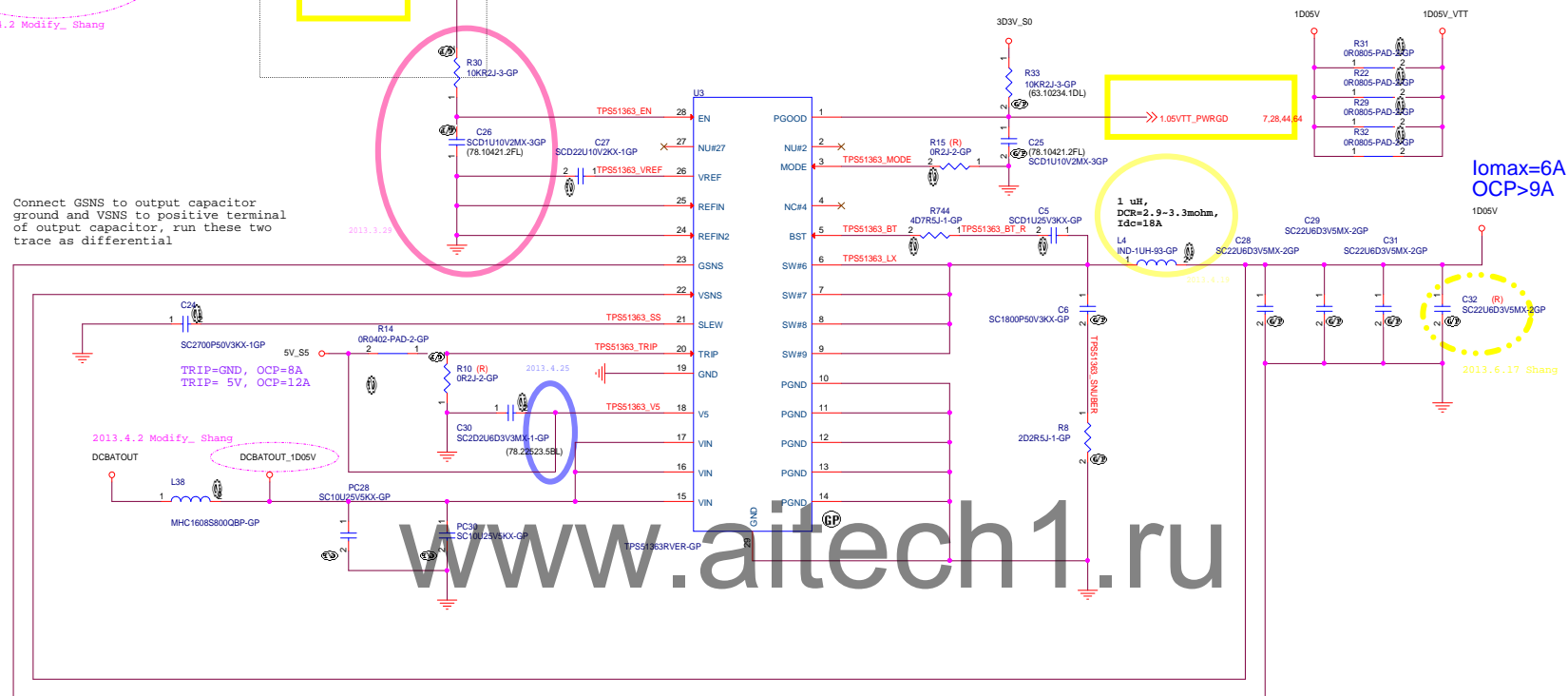
2013/07/22 1D05V\_VTT PWM EN->SLP\_S3# \_ RYAN

15,27,28,44,47,62,67

PM\_SLP\_S3#

Connect GSNS to output capacitor ground and VSNS to positive terminal of output capacitor, run these two trace as differential

2013.3.25



lomax=6A  
OCP>9A

2013/03/15 CHANGE POWER SOLUTION\_Ryan  
2013/04/01 Modify power schematic\_Shang

<Core Design>

緯創資通

Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taippei Hsien 221, Taiwan, R.O.C.

|                                 |                 |                        |        |
|---------------------------------|-----------------|------------------------|--------|
| Title                           |                 | 1D05V(TPS51363RVER-GP) |        |
| Size                            | Document Number | aPISA2                 | Rev 1A |
| Date: Thursday, August 29, 2013 | Sheet 65        | of 73                  |        |



## DDR 1D35V & VTT (TPS51363)





3D3V\_S5

PC3910 (G)  
SC10U6D3V3MX-GP

PC3911 (G)  
SC10U6D3V3MX-GP

PC3912 (G)  
SC10U6D3V3MX-GP

PC3913 (G)  
SC22P50V2JN-4GP

PC3914 (G)  
SC22U6D3V5MX-2GP

PC3915 (R)  
SC22U6D3V5MX-2GP

PC3916 (G)  
SC22U6D3V5MX-2GP

PC3917 (G)  
SC22U6D3V5MX-2GP

PC3918 (R)  
SC1800P50V2KX-1GP

PC3919 (R)  
SC1800P50V2KX-1GP

PC3920 (R)  
SC680P50V2KX-2GP

PC3921 (R)  
10KR2F-2-GP

PC3922 (G)  
10KR2F-2-GP

PC3924 (G)  
10KR2J-3-GP

RT8068\_Vin

RT8068\_VDD

RT8068\_EN

RT8068\_LX

RT8068\_FB

RT8068\_SNB

RT8068\_FB\_N2

PM\_SLP\_S3#

28.44,47.62,65,67

2013.4.19

2013.6.25

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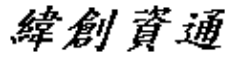




RESERVED

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<Core Design>

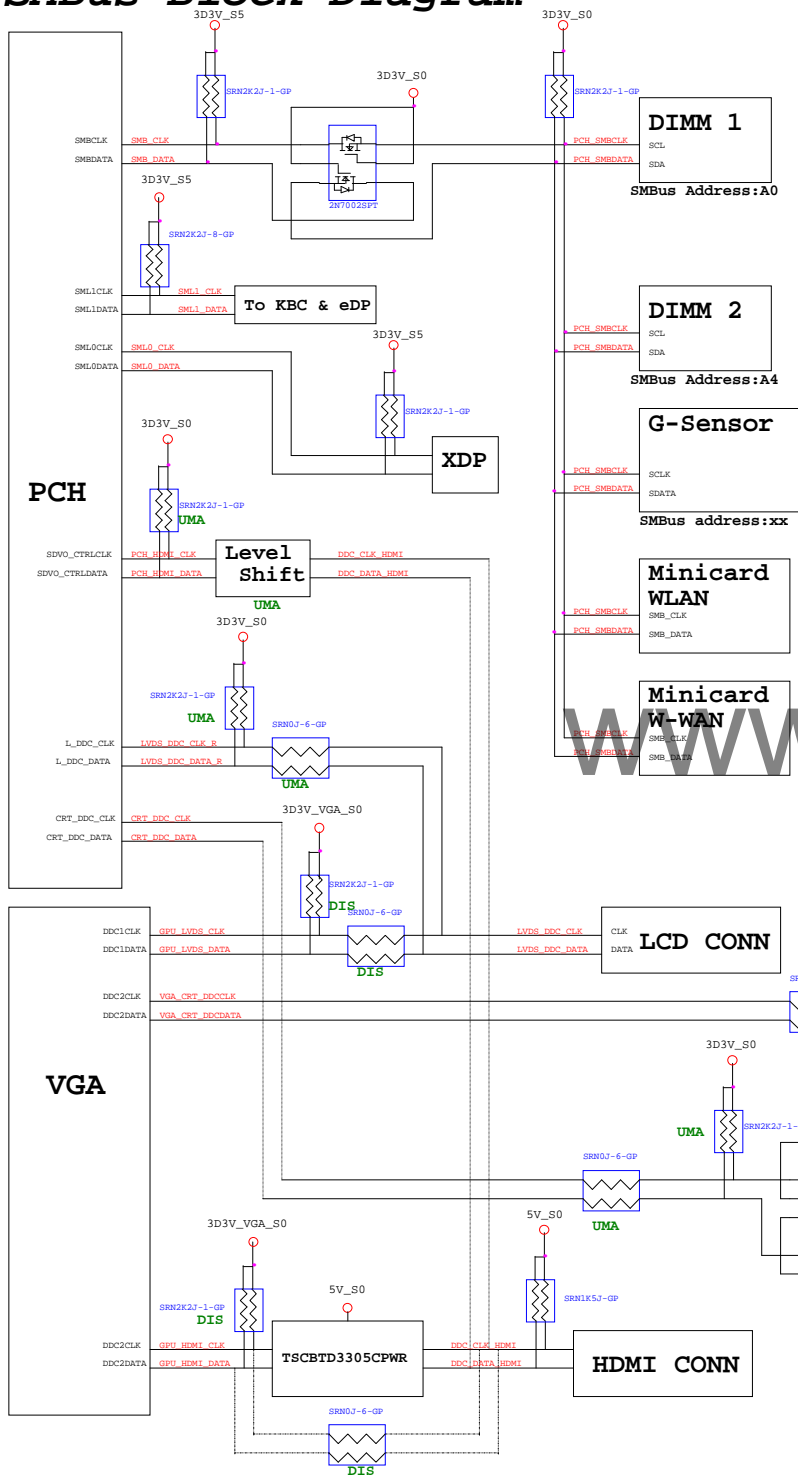
|                                                                                       |                                  |                                                                                                             |                  |
|---------------------------------------------------------------------------------------|----------------------------------|-------------------------------------------------------------------------------------------------------------|------------------|
|  |                                  | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                  |
| Title<br><b>RESERVED</b>                                                              |                                  |                                                                                                             |                  |
| Size<br>A4                                                                            | Document Number<br><b>aPISA2</b> |                                                                                                             | Rev<br><b>1A</b> |
| Date: Thursday, August 29, 2013                                                       |                                  | Sheet 68                                                                                                    | of 73            |



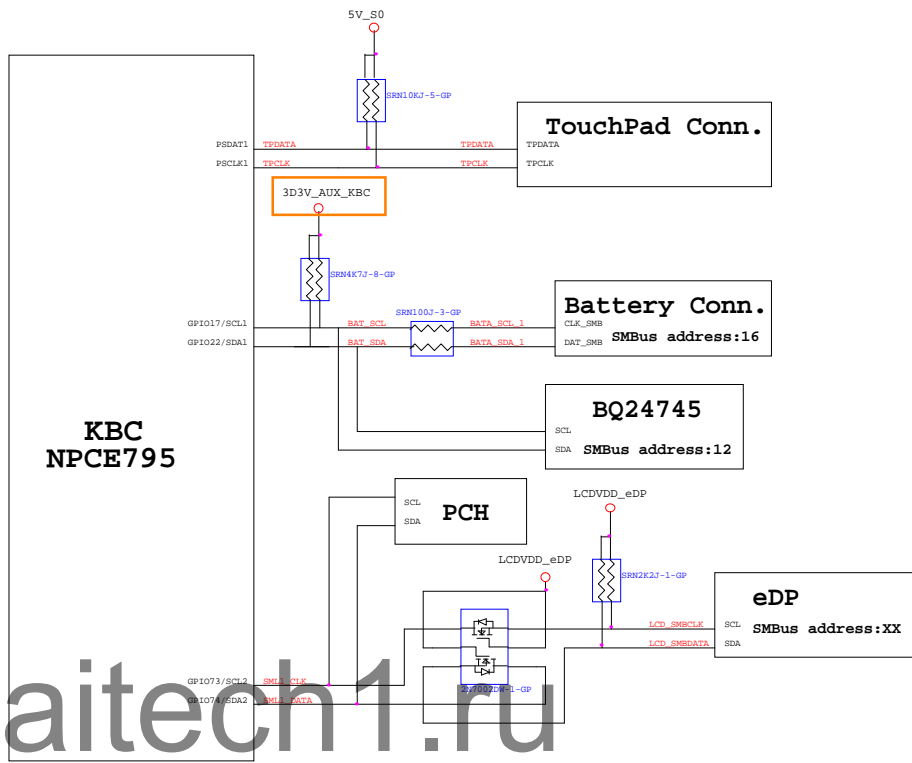




PCH SMBus Block Diagram

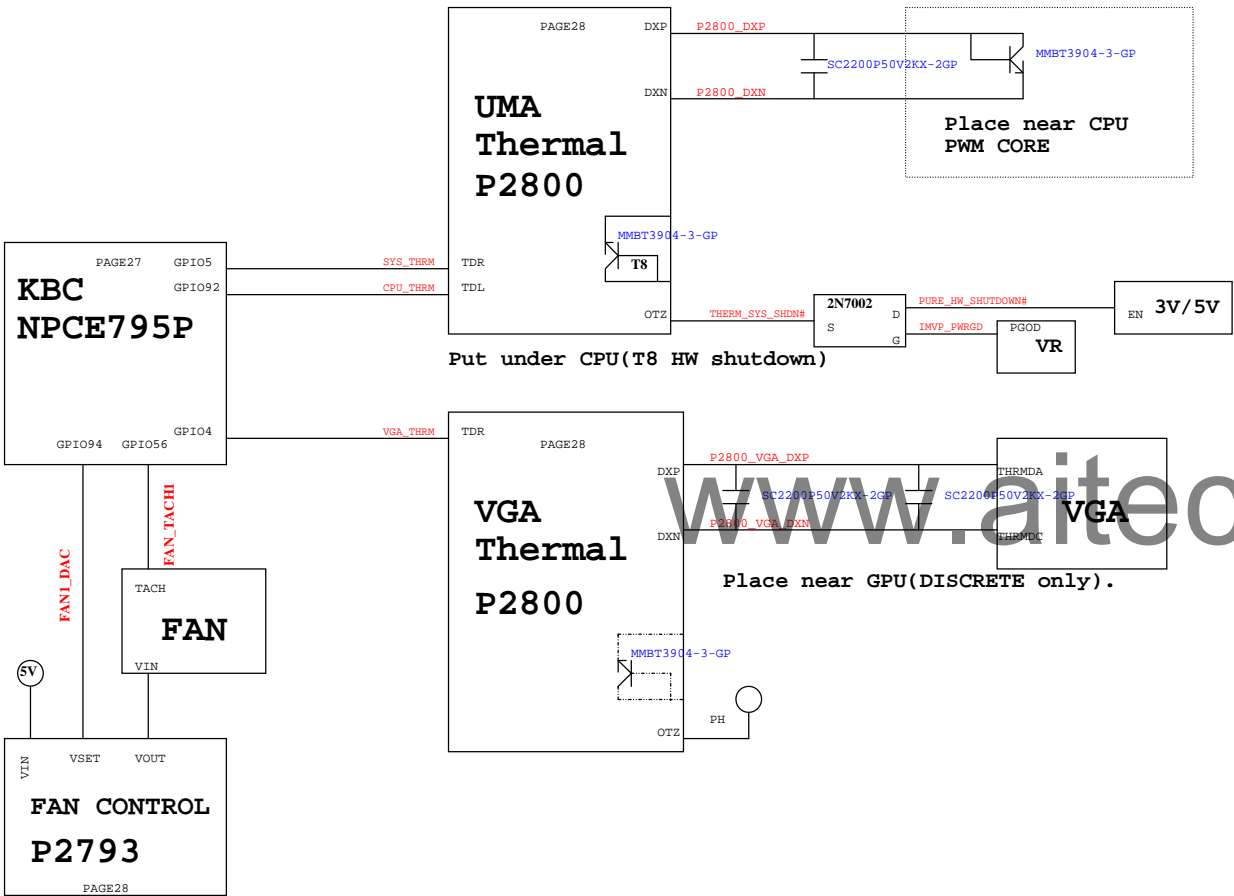


KBC SMBus Block Diagram

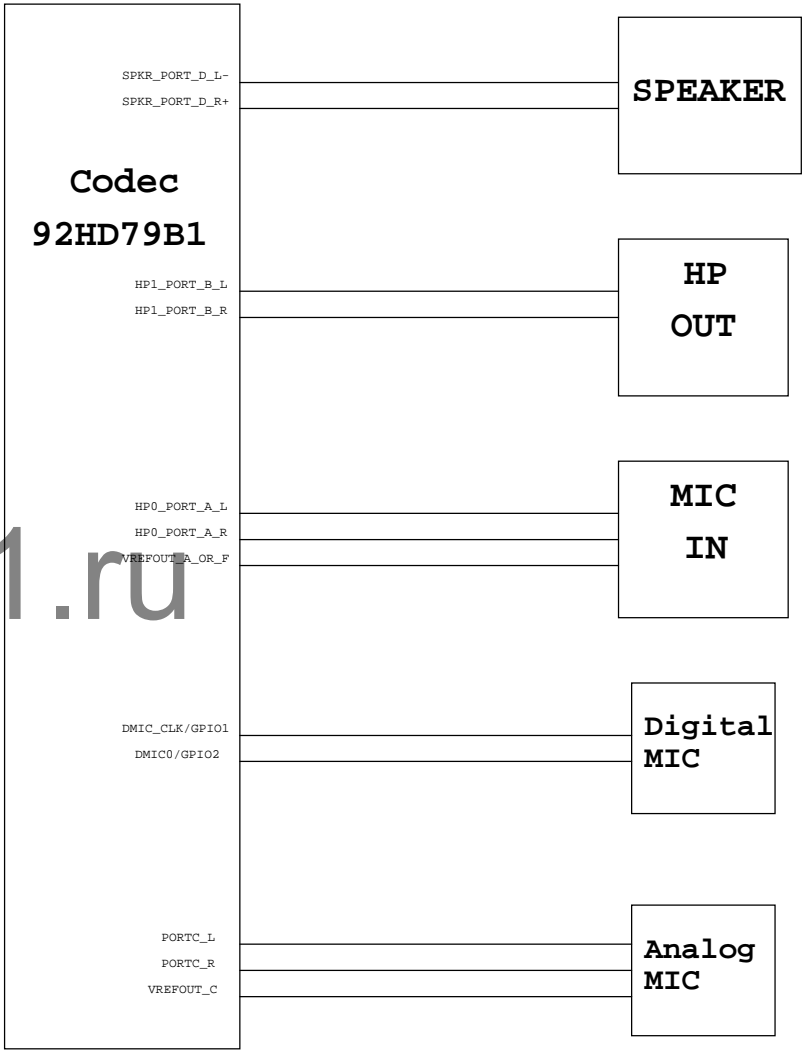




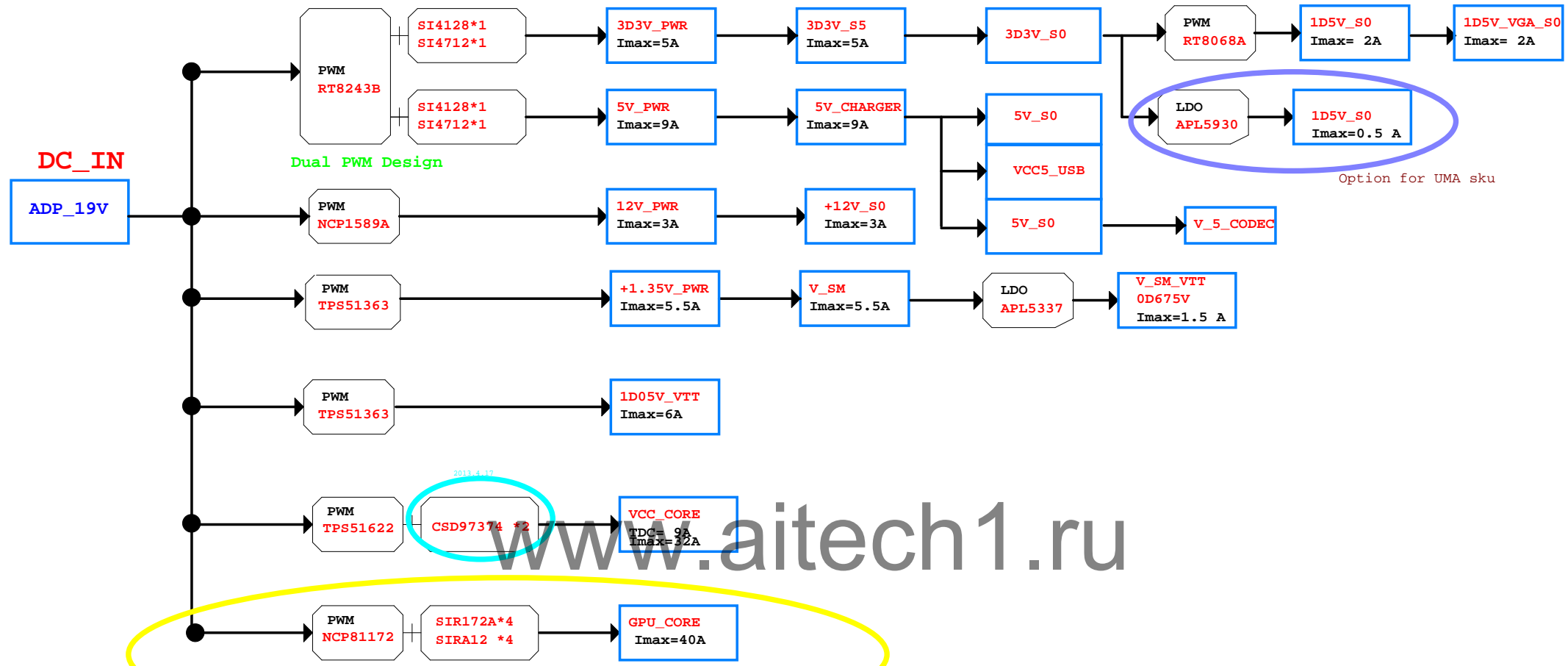
# Thermal Block Diagram



# Audio Block Diagram



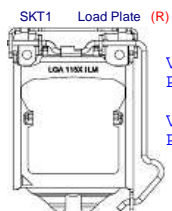






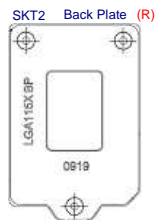
## Material part

### LGA115x CPU SOCKET Symbol



Vendor: LOTES  
P/N: 22.78003.011

Vendor: FOXCONN  
P/N: 22.78006.001



Vendor: LOTES  
P/N: 22.78002.011  
Thickness: max 2.2mm (含mylar及螺孔高)

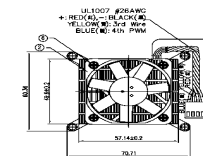
Vendor: FOXCONN  
P/N: 22.78006.011  
Thickness: 2.0mm (含mylar)



Vendor: LOTES  
P/N: 22.78005.171

Vendor: FOXCONN  
P/N: 22.78005.161

### HeatSink+FAN Symbol



Vendor  
P/N:

HSFAN1  
(R60.3KN01.001)

### LABEL



LBL1  
LABEL  
(45.41107.011)

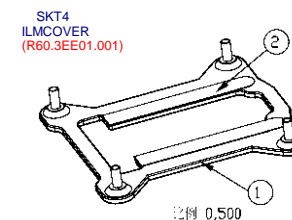
MB serial NO# and MAC address  
45.41101.001 -> 35 x 15mm  
45.41107.011 -> 70 x 8mm



LBL2  
LABEL  
(R)



LBL3  
LABEL  
(R)

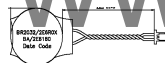


Vendor: LOTES  
P/N: 22.78005.171

Vendor: FOXCONN  
P/N: 22.78005.161

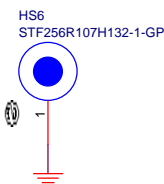
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### Stand-off



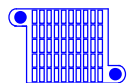
BAT1  
BATTERY CR2032\_30MM  
(R23.21221.024)  
Wire Length: 30mm

Vendor  
P/N:  
23.21221.024  
23.21212.031



34.3KF01.001 for 5.2mm slot 62.10043.G11  
34.3HJ03.001 for 9.0mm slot 62.10043.E41

### HeatSink Symbol



HS8  
HEATSINK  
(R60.3ET05.001)

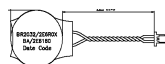
Vendor  
P/N:  
60.3ET05.001  
60.3ET05.011  
60.3ET05.021

### Battery Symbol



BAT3  
BATTERY CR2032  
(23.20068.001)

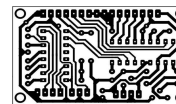
Vendor  
P/N:  
23.20068.001  
23.20023.311  
23.22063.001




BAT2  
BATTERY BR2032\_60MM  
(R23.24220.612)  
Wire Length: 60mm  
耐高溫>85C

Vendor  
P/N:  
23.21208.061  
23.24220.612

### PCB Symbol



PCB1  
PCB  
(R)

|                                                                                       |                               |                                                                           |        |
|---------------------------------------------------------------------------------------|-------------------------------|---------------------------------------------------------------------------|--------|
|  |                               | <b>Wistron Incorporated</b><br>12F, 88, Hsin Tai Wu Rd<br>Hsichih, Taipei |        |
| Title <b>HeatSink / Battery cell /etc</b>                                             |                               |                                                                           |        |
| Size B                                                                                | Document Number<br><b>TBD</b> |                                                                           | Rev 1A |
| Date:                                                                                 | Thursday, August 29, 2013     | Sheet 73 of 73                                                            |        |